TECHNISCHE HOGESCHOOL TWENTE

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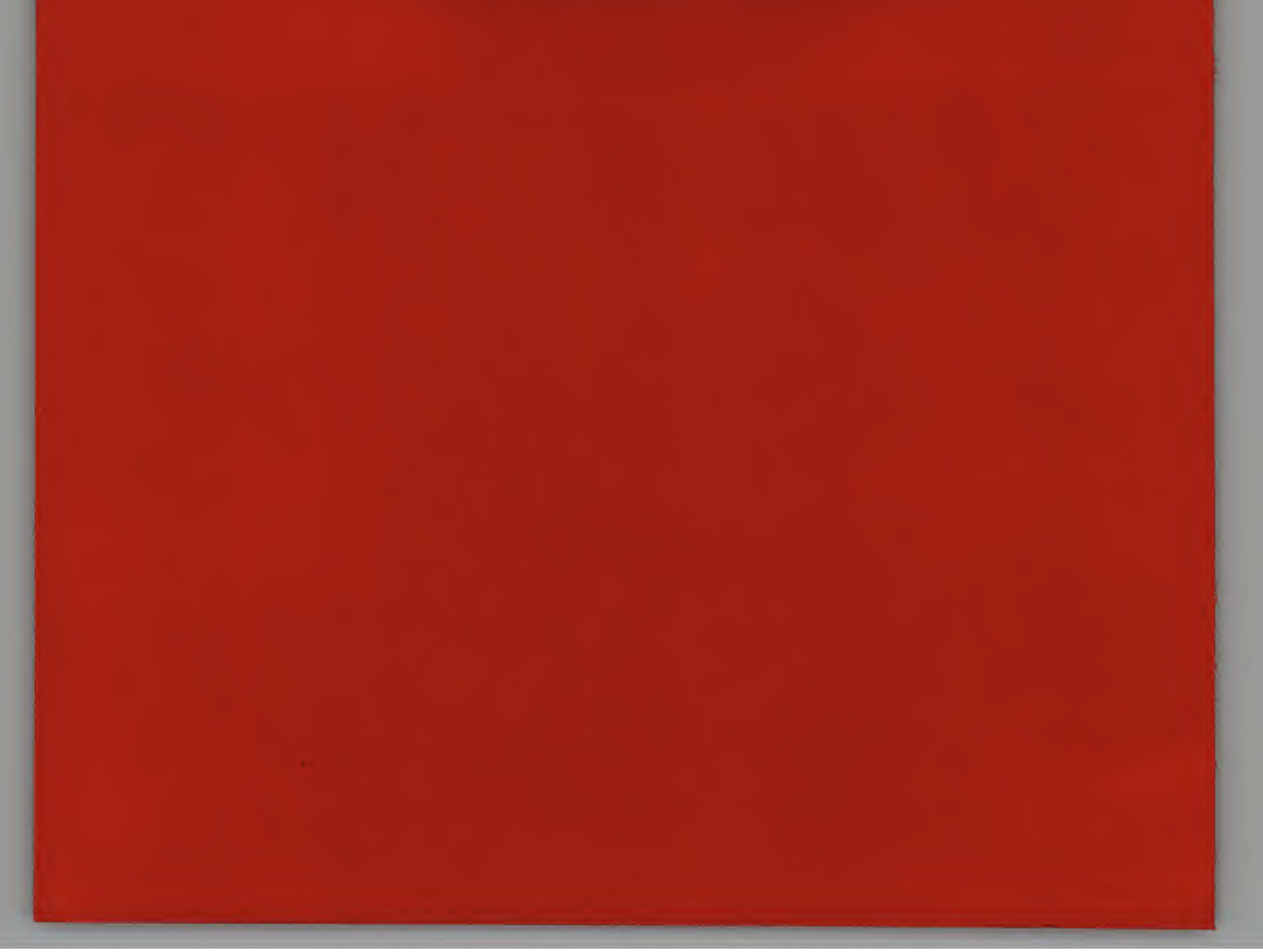

MICROFLOPPY

COMPUTER MANUAL

SERIAL NUMBERS 135-299

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Very respectfully,

William Noyce
Vice-President-Marketing

WN/lmp

PREFACE

Charles River Data Systems started as a manufacturer of mainframe computer memory systems. The company later diversified into the manufacture of add-on peripherals for the PDP-11 family of processors made by Digital Equipment Corp. The CRDS FD-11 dual floppy disk drive system is a completely hardware and software compatible floppy system for the PDP-11.

The advent of the LSI-11 family of products has made the power and architecture of the PDP-11 system available to the small system user. With the technology developed in the FD-11 system and the expertise in computer systems available at Charles River Data Systems, a complete computer system became the natural extension of the product line.

The MICROFLOP 11 (MF-11) system is completely software compatible with the Digital PDP-11V03 system. It will, for example, run the RT-11 operating system without modification. It includes several standard features not found in the PDP-11V03 system such as individual unit write-protect, the capacity to format a diskette, run self-test diagnostics on the drive system under microprogram control, and hardware bootstrap.

The complete MF-11 system will accept any standard DEC module for the LSI-11. It provides a cost-effective tool for small business, laboratory, and educational applications.

This manual will provide you with all the details needed to unpack, install, and use the MF-11 system. Please read the instructions completely and carefully before attempting to use it.

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INTRODUCTION

1.1 GENERAL

The Charles River Data Systems MF-11 computer system is an integration of the Digital LSI-11, the CRDS FD-200 floppy disk controller, dual floppy disk drives, and a custom power supply in its own enclosure.

The MF-11 is available with either a four slot standard backplane or an extended eight slot backplane. The two versions differ only in enclosure dimensions, number of cooling fans, and backplane capacity; this manual applies to both configurations.

1.2 SCOPE OF MANUALS

The following documentation is included with your MF-11 System:

MF-11 Manual (you are reading it)
Digital Microcomputer Handbook, Second Edition
LSI STOR-11 pamphlet (if you have ordered expansion memory)

The MF-11 Manual is intended for use with the DEC Microcomputer Handbook. This manual will supply details for the unpacking, installation, and use of the MF-11 system, describe the floppy controller and drives, and give details and specifications for the power supply. Details and specifications for the LSI-11, DLV-11, and other DEC modules are contained in the Microcomputer Handbook. Details and specifications for LSI-STOR 11 extension memory are given in the pamphlet supplied.

1.3 SYSTEM CONFIGURATION

MF-11 Systems consist of the following:

1	H9270 Quad Backplane or Extended Backplane
1	LSI-11: KD-11F CPU with 4K on-board memory
2	Shugart SA800-series Floppy disk drives
1	FD11-200 Controller Card with bootstrap option
1	Power Supply
1	Enclosure
1	Front panel with indicators and controls

Options Include:

IN 1611 add-on memory (up to 24K on a single 22.8 x 13.2 cm module) in increments of:

8K
16K
24K

DLV-11 Serial interface and cables (EIA RS-232 or 20 ma current loop)
DRV-11 Parallel interface

1.3 SYSTEM CONFIGURATION; OPTIONS (Continued)

KEV-11 Extended Arithmetic Instruction PROM
Any other standard DEC module for the LSI-11.
RT-11 Version 2C or Version 3 Operating System
Fortran IV
BASIC-11
FOCAL
APL
Scientific Subroutine Package for Fortran

RSX-11S Operating System

The system can be wired to accept either 110 v/60 Hz, 220 v/50 Hz, or 110 v/50 Hz. It is available with slides for rack mounting, or with rubber feet for desk-top use. Wiring is a factory installed option. All others are field or factory installed.

SYSTEM OVERVIEW

2.1 SYSTEM COMPONENTS

The two major components of the MF-11 are the Central Processor and the Floppy Controller. Typically, the floppy drive system will provide the only secondary storage on the system. The interplay between these devices should be well understood by the user before attempting to make design decisions involving the interface of other modules to the system.

This will aid in the determination of transfer type, interrupt priority selection, register location, and other considerations.

2.1.1 KD11-F CENTRAL PROCESSOR UNIT

The standard processor supplied with the MF-11 system is the KD11-F version of the Digital LSI-11. It is a sixteen-bit machine, featuring direct addressing of 32 K 16-bit words, byte addressing, an asynchronous bus, hardware memory stack, DMA capability, vectored interrrupts, and a powerful instruction set. The KD11-F also includes 4K words of on-board RAM and a microcode control program in ROM, ODT (On-line Debugging Technique).

Complete descriptions of the KD11-F are contained in section 4.2 of the Digital Microcomputer Handbook. Chapter 3 of the same book describes the LSI-11 bus. The Handbook will also detail the use of the ODT program, the processor instruction set, and specifications for DEC modules.

2.1.2 FD11-200 FLOPPY DISK CONTROLLER

The controller card contains all the electronics involved in the dual disk system except the read/write circuits in each drive. It is based on the 8080 microprocessor, which controls all reading from and writing to the disk drives, follows the IBM 3740 format in disk operations, and emulates the instruction set of the Digital RX11 floppy disk system.

The FD11-200 card plugs into one Small Peripheral Controller Slot (SPC) in the backplane. It will work with any LSI-11 system. A 50-conductor ribbon cable is used to daisy-chain the two disk drives and connect them to the controller card. A twisted pair of 18 gauge wire connects to the power supply. (See Figure 2-1).

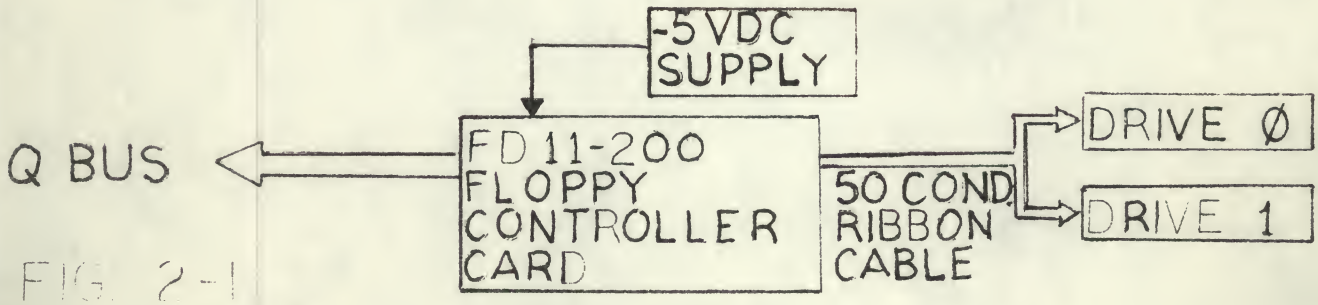


FIG 2-1

2.1.2 FD11-200 FLOPPY DISK CONTROLLER (Continued)

The FD11-200 transfers data under CPU control, byte by byte, to and from an internal 128 byte buffer. Transfer speed is limited by the 8080 to about 18 microseconds per byte. All other disk functions are under the control of the 8080 microprocessor, freeing the LSI-11 central processor for other duties (the CPU issues commands then runs another process until an interrupt occurs at completion of the disk operation). The 8080 program also provides full emulation of the RXV11 instruction set. This system of disk control takes full advantage of the LSI-11 interrupt processing structure and the existing efficient software device handlers written for floppy disk on the LSI-11.

2.1.2.1 BOOTSTRAP

The FD11-200 card also contains a read-only memory which responds to bus addresses 173000 to 173776, the first 32 words of which contain a bootstrap routine. This routine is automatically executed on power--up and at the press of the INIT key, as long as the system is in the ENABLE state. The bootstrap may be used in combination with ODT to bootstrap unit 1 as well as unit 0. The bootstrap feature is a strappable option, and may be removed if the area of memory it fills interferes with user needs.

2.1.2.2 INSTRUCTION SET

The instruction set of the FD11-200 contains several extensions to the RXV11 instruction set. Complete details of the instruction set are given in chapter 5 of this manual.

2.1.3 OPTIONAL INTERFACES

Additional cards may be bought or built for interfacing the MF-11 system to peripheral devices. The DLV-11 serial interface (see Microcomputer Handbook, section 4.8) is used for interfacing console terminals, modems, and other serial lines at speeds up to 9600 baud (or externally clocked rate). The DRV11 (Handbook, section 4.10) is a general purpose parallel interface. These cards will fill the majority of user requirements.

Additional interfaces are available for IEEE instrument bus, A/D and DAC, and so on. Any user constructed interface needs only to have sufficient circuitry for interface to the LSI-11 bus, or be built around a bus foundation card to work with the MF-11 system. Full documentation on interface requirements is available. The Handbook, chapter 4, describes the bus foundation card (DRV-11P) and other standard interfaces.

2.1.4 OPTIONAL MEMORY

The LSI-11 is capable of direct addressing of up to 28K 16-bit words of RAM. A single half-height module can be ordered from CRDS which will in combination with the CPU's on-board RAM bring the system memory to this total.

Most general applications will require at least 8K words to support an operating system, and 12 to 16K is desirable for applications involving software development.

2.1.5 BACKPLANE AND POWER DISTRIBUTION

The standard 4-slot backplane is large enough to support one LSI-11, a console interface, 24K of expansion memory, the FD11-200 Disk Controller and two more serial interfaces (or equivalent).

The expanded 8-slot backplane has four full slots more, enough for eight more serial interfaces or four more disk controller cards. The backplane used does not require any interface modules or cabling to connect two banks of four slots each, as in a system employing a standard backplane and an expansion box; eight full slots are supplied for the user.

A multiple voltage power supply mounted as a single unit provides the 5 volt and 12 volt dc sources from which all required power in the system is taken. Chapter 6 of this manual describes and specifies the power supply.

2.1.6 FRONT PANEL CONTROLS

The MF-11 System front panel controls provide for control of AC power, initializing the system, moving it between halted and running states, and selective enabling of the Line Time Clock (LTC). Functions normally associated with a programmers console, such as examination and modification of memory from the console indicators and switches, are provided by console emulation routines in the ODT monitor. These routines are entered whenever the processor is in the halted state.

2.2 MEDIA

The magnetic medium employed by the MF-11 is the familiar diskette, or floppy disk. The flexible diskette consists of a mylar disk coated with an oxide and encased in a plastic jacket. The jacket is lined with a fiber material which cleans the disk as it rotates. In use, the jacket is held fixed in the drive while the disk rotates.

2.2.1 COMPATIBILITY

The MF-11 is designed to be compatible with IBM's 3740 format, the format also used by DEC's RX11. This format is used by many manufacturers, providing something of an industry standard. For this reason, diskettes written on an RX11 system may be read by the MF-11 and vice-versa. Complete compatibility and interchangeability of diskettes is maintained.

2.2.2 IBM FORMAT

The IBM 3740 Data Entry System defines a format wherein each disk contains one index track (numbered 0), 73 record tracks (01 through 73), two alternate tracks (74 and 75) and one spare (76). Each track is divided into 26 sectors which contain from one to 128 8-bit data bytes. The organization of sectors on a track is determined logically from records written on the diskette (soft sectoring) rather than through mechanical means (hard sectoring). Diskettes are usually supplied with the sectoring information already written on the diskette; normal use of the medium will change only the data fields in each sector. The principal characteristics of the format are shown in Figure 2-2.

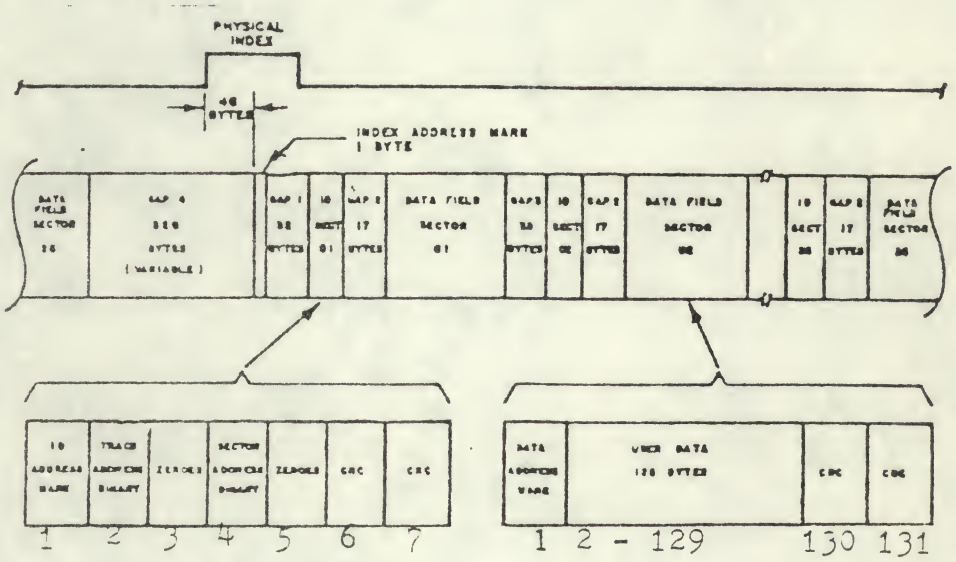


Figure 2-2

2.2.2.1 CYCLIC REDUNDANCY CHECK (CRC)

Every data field and ID field on the disk has a pair of CRC bytes appended to it. These bytes, which are generated by the controller and written as the field is written, represent a cyclic permutation of all the data bits in the field, from bit 0 of the address mark to bit 7 of the last byte in the field (excluding the CRC bytes). As data is read by the disk system, the hardware will regenerate and compare the CRC bytes, returning an error condition to the software when the CRC written out with data does not match the CRC calculated for that data (CRC error), or when the CRC of an ID field as written on the diskette fails to match the CRC generated in the controller while reading it (CRC on header error).

2.2.2.1 CYCLIC REDUNDANCY CHECK (continued)

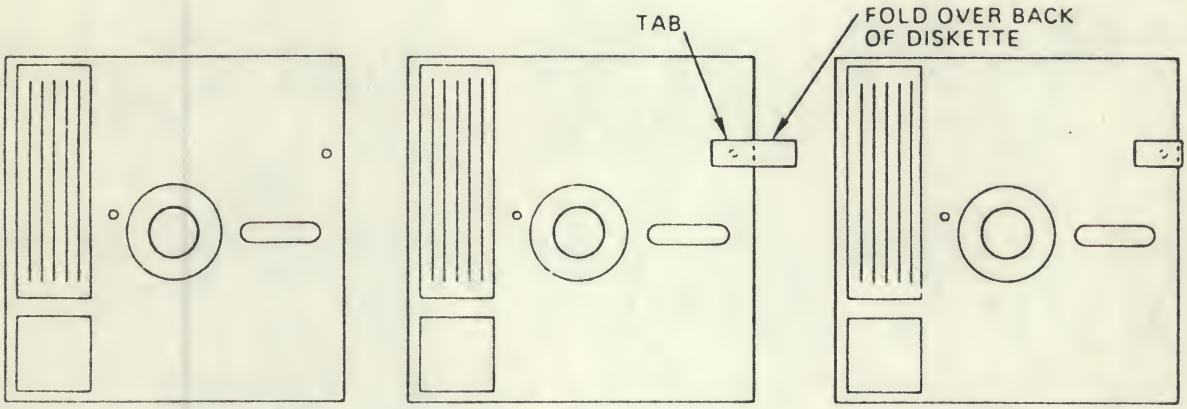
The cyclic permutation is the remainder that results from dividing the data bits (represented as an algebraic polynomial) by a generator polynimial, G(x). The function used in the IBM format described above is:

$$G(x) = x^{16} + x^{12} + x^{5} + 1$$

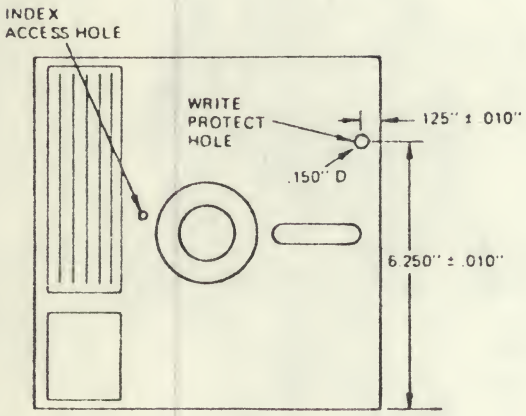
2.2.3 WRITE-PROTECT FEATURE

The ability to write protect diskettes is provided by a photocell and LED combination in the disk drive. The photocell senses the presence or absence of a write-protect hole in the diskette jacket. A diskette without a hole is not write protected (standard IBM supplied diskette). Placing a hole in the diskette as shown in figure 2-3 will prevent writing on the disk. Covering this hole with opaque tape will again enable writing. Some manufacturers will supply diskettes with a write-protect hole or notch cut into the diskette; there are usually write enable tape strips packed with pre-cut diskettes for the purpose of write-enabling the media. These strips are usually of the peel-and-stick variety. Black electrical tape makes a good substitute for these strips.

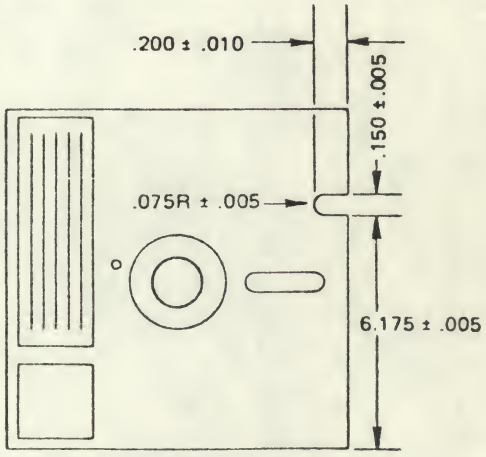
It should be noted that unexpected write operations may occur on a system disk (writes which you do not explicitly request). For example, under RT-11, the USR may swap unexpectedly, writing the contents of some memory out to the system swap blocks. A write-protected system disk may cause a system crash in this situation. The write-protect feature must be used with care, and should be avoided on an RT-11 system device.



Diskette Write Protected



Write Protect Hold Specifications



Write Inhibit Notch (Optional)

Figure 2-3

2.3 DISK SYSTEM SPECIFICATIONS

Capacity

Bytes per sector:	128
Sectors per track:	26
Tracks per diskette:	77
Total bytes per diskette:	256,256

Access time and transfer rates

Diskette to controller buffer:	32 microseconds/byte
Buffer to CPU:	16 microseconds/byte
Track to track seek:	6 milliseconds
Head settle time:	14 milliseconds
Rotational speed:	360 RPM $\pm$ 2.5%
Average access (25 track seek + rotational latency):	320 milliseconds

Recording technique

Method:	Double frequency
Bit density:	3200 bpi
Track density:	48 tracks per inch
Surfaces used:	1

Reliability

Seek error rate:	1 in 10^6 seeks
Soft read error rate:	1 in 10^9 read operations
Hard read error rate:	1 in 10^{12} read operations

2.4 ENVIRONMENTAL REQUIREMENTS

Temperature range

MF-11, operating:	50 to 100 deg F
MF-11, storage:	32 to 150 deg F
Diskette, storage:	50 to 125 deg F

Humidity: 10 to 80 percent, without condensation

Electrical

Input: 120 VAC, 60 Hz, at 4 amps

Physical (Enclosure dimensions)

Standard backplane:	10.5 x 17.0 x 18.0 in
Extended backplane:	10.5 x 17.0 x 22.0 in

UNPACKING AND INSTALLATION

3.1 Unpacking

The MF-11 is shipped complete in a single carton. The carton must be opened from the top (printing on sides of carton reading properly). Remove the slides, manuals, cables, and any modules from the green packing material. The top section of the packing material may now be removed, exposing the MF-11 chassis. Reach down through the cut away sections to each side of the chassis, grasp the unit from the bottom and lift it up and out.

3.2 Module and Cable Installation

Most units are shipped with all modules installed and cables brought out to the rear of the unit. If there are any additional cables to attach, or separate modules to be installed, it will be necessary to remove the top cover from the enclosure.

The top cover is secured by three screws along each edge on the top, and six screws on the back. Remove all screws (not the four power supply mounting screws placed on the side panels) and remove the cover. Access is then given to the backplane.

Modules will be shipped factory wired to customer specifications. If the module requires changes in configuration or is a user supplied module, refer to the Handbook "Installation" section, chapter six, for a checklist and cross-reference (or other manufacturers specifications as appropriate).

Unless otherwise specified by customer, the standard MF-11 is configured thus:

KD11-HC Processor Jumpers

Power up mode 2: the bootstrap at location 173000 will be executed on power up if the processor is ENABLEd. ODT is run if the processor is in the HALT state.

On board RAM is enabled and configured for the low 4K of memory.

LTC interrupts are enabled

Memory expansion boards

Set to provide contiguous memory (4K-top of memory)

DLV11 Console interface

device address 177560
vector address 60
FEH installed (framing error halt--BREAK causes halt state)
300 baud
EIA and 20 milliamp current loop options active (interface cable selects which is used)

3.2.1 Module Placement Considerations

The CPU board must occupy the first slot of the backplane (as shipped). Two signal lines which handle interrupt request and grant protocol are daisy-chained through the other modules in the backplane. This protocol gives devices physically nearest the processor the highest interrupt priority. This system prohibits empty backplane slots between the processor and an interrupt driven device interface. (See Handbook, section 1, paragraph 6.3.)

In general, devices requiring time-critical interrupt service, such as high speed modems which will lose data if it is not processed before the next character is received, should be placed closer to the CPU than devices which operate with low speeds or buffers. Memory and other devices which never require interrupt service should be placed farthest from the CPU.

The FD11-200 controller card is shipped in slot two, but will work in any slot and may be repositioned if desired.

3.2.2 Module Insertion

Insert modules along the card edge guides. Apply force to the handles when card edges are lined up with backplane slots. Considerable force may be required to seat the card. (See Handbook, section 1, paragraph 6.4 for cautions and handling instructions.)

3.2.3 Cabling

Most devices connect to a 40-pin BERG connector or equivalent at the interface card. All cables should be brought out through the rear of the chassis, positioned to fit under the notch provided in the top cover. See the instructions in the Handbook for each module, or consult the manufacturer's data sheet if you are unsure which cable to use for a given device.

If using the unit in a table-top configuration, skip section 3.3.

3.3 Rack Mounting

First separate each slide into two pieces by pulling them apart. It may be necessary to release the safety catch button inside the slide section depending on the direction in which they are pulled apart.

The slide sections with right angle ears should now be mounted as shown in figure 3-1. In order to exactly fit the MF-11 into a 10½ inch section, it is necessary to count off 4 holes above the section below. The slides are mounted by screwing two 10-32 machine screws through the slides, cabinet mounting holes, and into a tapped retainer plate, clamping each slide section in front of the cabinet's mounting rail as shown in figure 3-2. The retainer plate is not required if the cabinet mounting holes are tapped for 10-32 hardware.

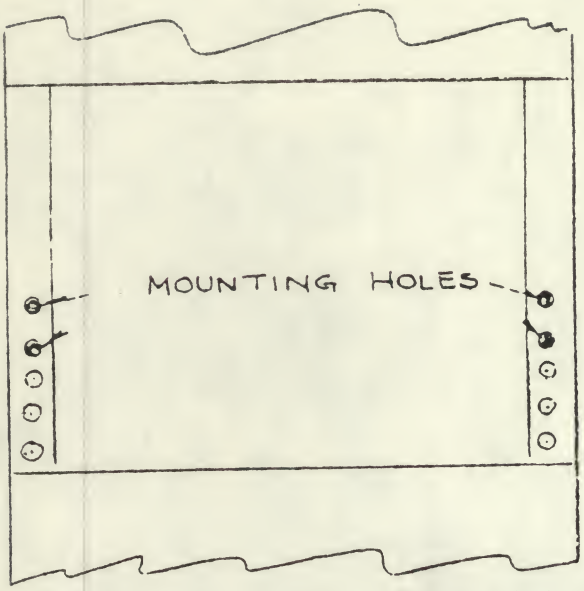


Figure 3-1

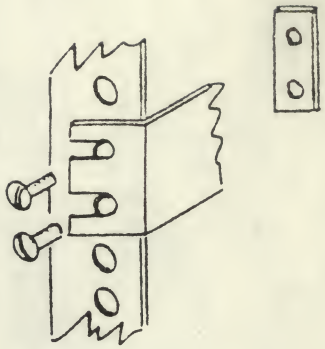


Figure 3-2

Two right angle rear mounting brackets have been supplied for attaching the slides to the rear mounting rail of the cabinet. First mount the two brackets to the rear mounting rail in the same fashion that the front ears of the slides were attached. Use two 10-32 screws and retaining plates if necessary.

The brackets should then be attached to the slides using one 10-32 machine screw and one 10-32 kep hex nut on each slide. The hex nut must be kept on the outside of the slides.

The remaining slide sections may now be mounted on the MF-11 chassis. Use six 10-32 machine screws, three on each side, attaching the slides as shown in figure 3-3.

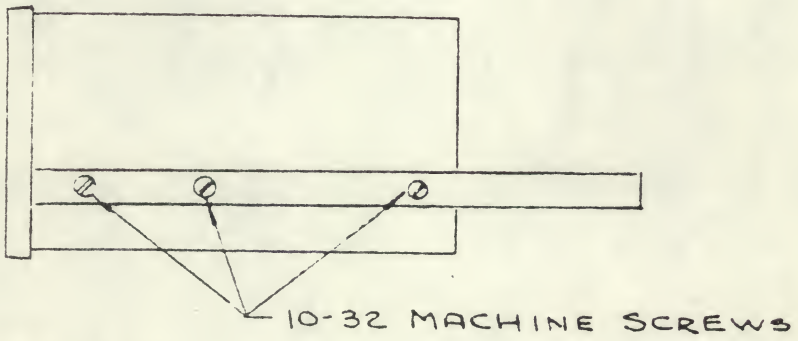


Figure 3-3

The MF-11 may now be installed by lining up the two slide sections and mating them. After pushing in a short distance, the safety catches must be pressed in to allow the unit to travel all the way back into the cabinet.

3.4 Electrical Connections

The MF-11 should be connected to the same grounded AC electrical system as all peripherals attached to it, using properly grounded three wire receptacles. If power connections fail to meet this constraint, a potential may develop across system wiring and cause damage to peripherals and interface cards.

3.5 Initial Checkout

The following procedure should be followed to verify proper installation of the system:

1) Power up the console terminal.

2) Place a scratch diskette in each drive and close the doors.

3) Set the ENABLE/HALT switch to HALT.

4) Power up the MF-11 by turning the power switch ON.

5) The DC OK lamp should come on. Both drives should now calibrate themselves. First unit 1 steps out 10 tracks and then steps in track by track until the drive signals track 0 has been reached. This procedure is then repeated on unit 0. At the completion of calibration, the head on drive 0 is loaded and sector 1 of track 1, unit 0 is read into the controller buffer. The head load is indicated by the red activity LED in the door open lever, which should remain on for about one second after the read is finished.

   If this fails to happen, check the seating of the controller card, drive cabling, and -5 volt power connection to the controller card. The LED near the connector on the FD11-200 card indicates the presence of the -5 volt supply.

6) Read the FD11-200 control and status registers with ODT:

   @177170/ 000040 (line-feed) (user input is underlined)

   @177172/ 000204

   See chapter 5 for the meaning of these bits.

7) If these procedures work properly, the system should be ready for use. Follow the instructions given for bootstrapping the system given in chapter 4. Run diagnostics or an operating system as you wish.

The most common cause of apparent failure is a loose connection to the console terminal at the interface card. If the DC indicator is on and everything

operates as described but no output appears on the terminal, check the cabling. Also verify that the options on the DLV11 and the cable used match the type of terminal in use (especially in baud rate).

Also check that you are not using write enabled media if you find that a system bootstraps properly and then fails repeatedly in use.

Call the factory for assistance if you find the equipment defective. Obtain a return authorization before shipping material back to the factory.

INSTRUCTIONS FOR USE

4.1 Differences between MF-11 and PDP-11V03

Instructions for use of the MF-11 system are identical to those given in Section 2 of the Handbook for operation of the LSI-11 and RXV11, noting the following differences and options:

1) The bootstrap routine starting at location 173000 is provided by ROM on the FD11-200 floppy disk controller card; there is no REV11 module installed in the system.

2) Front panel indicators and controls are as described below.

3) The standard console device configuration (DLV11 has FEH, framing error halt, installed) allows entry to ODT by use of the BREAK key.

If you have not used floppy disk media before, please read paragraph 4.5 and following on the handling of diskettes before using the system.

4.2 Front Panel Controls

Power Switch

A two position rocker style circuit breaker which controls all power to the MF-11. Units wired for 220 volt operation will have a fuse wired in series with the switch. Note that there is no separate AC or DC switch on the power supply or rear of the unit as in the PDP 11/03.

INIT Key

A momentary contact, spring return switch. When pressed down, this key causes the sytem to initalize all devices on the bus and execute the power-up sequence. This key can be used to recover from system crahes or reset the hardware when executing from ODT. The response of the system to INIT is dependent on the setting of the ENABLE/HALT switch.

ENABLE/HALT SWITCH

A two position toggle switch. When placed in the ENABLE (up) position, the processor is able to execute programs from memory. If an INIT takes place with this setting, the automatic bootstrap sequence will be executed. When placed in the HALT (down) position, the processor is in the halt state, and executes the ODT microprogram. The switch may be used to stop program execution at any time by moving it from ENABLE to HALT. Note that moving it back to ENABLE will not cause the program to continue until you issue the proceed (P) command to ODT. Further, if the processor is HALTed with this switch, the proceed or go (G) commands

will simply display the new program counter value and not start execution.

LTC Switch

The LTC switch is a two position toggle switch for enabling and disabling line time clock interrupts. When in the OFF (down) position, clock interrupts will not occur. It is necessary to switch the LTC off to run some programs, notably the RXDP diagnostics, which cannot handle clock interrupts. The switch must be ON (up) for normal operation of RT-11 and similar systems which use the LTC as a system clock.

4.3 Bootstrapping the System

With a system disk installed in drive 0, and the ENABLE/HALT switch set to ENABLE, the system will be booted on power up or whenever the INIT key is pressed. If the LTC is OFF, the system may be bootstrapped from ODT by typing:

@173000G (user input is underlined)

The LTC is switched off to disable interrupts before the monitor is installed to handle them. Pressing INIT while in the HALT state will also provide protection from this problem.

4.3.1 Bootstrapping from Drive 1

To bootstrap the system from unit 1 (a BOOT monitor command may also be employed if a system is running), place a system disk in drive 1 and close drive door. Set the ENABLE/HALT switch to HALT. Press INIT. After both drives have calibrated, type the following commands to ODT:

@R 2/ 000000 20 (return)

Set the ENABLE/HALT switch to ENABLE. Continue with:

@173002G

Drive 1 will be bootstrapped (the RUN light should come on).

4.4 Indicators

RUN

This lamp should follow the state of the processor, lit when executing from program memory and out when in the HALT state. If the RUN lamp goes off while the processor is ENABLED and running, it generally indicates that a software crash has occurred. Note that it provides an indication of the halt state when switching from HALT to ENABLE and that it will come on when a valid proceed or go command is issued. Some flicker of the lamp when executing an INIT or power-up is normal.

4.4 Indicators (continued)

DC OK

This lamp should follow the on/off setting of the power switch. If the system will not come up and this lamp is off a power supply failure is indicated.

4.5 Diskettes

Diskettes must be treated with care to prolong media life and protect data recorded on the sensitive surface. In addition, experience has shown that not all of the media available is of good quality. We have found that the manufacturers listed below have good quality control on the production of their diskettes:

IBM
ITC 9000 series
Dysan

Read errors on diskettes are often the result of bad media; we therefore cannot be responsible for the performance of the MF-11 with other brands. Manufacturers are evaluated on the life of the diskette, the accuracy of the formatting information and the head wear caused by the diskette. Contact the factory for updated approval list if you are in doubt about a particular brand of media.

4.5.1 Diskette Care

The following rules should always be followed when handling diskettes:

1) Always return the diskette to its envelope after use.

2) Do not place any object on top of diskettes stored horizontally.

3) Observe the storage temperature and humidity specifications of the diskette manufacturer and store them at opertaing ranges whenever possible.

4) Do not write on the disk jacket or labels affixed to the disk jacket unless using a felt-tip pen.

5) Apply only labels of the peel-and-stick variety to the disk.

6) Do not touch the recording surface through the read/write aperture in the disk jacket.

7) Do not store diskettes in dusty areas.

8) Never clean the diskette.

9) Never expose the diskette to prolonged heat or sunlight.

4.5.2 FORMATTING A DISKETTE

WARNING: EXPOSED AC: USE OF THIS ROUTINE REQUIRES OPERATION OF THE MF-11 WITH THE COVER REMOVED. AVOID CONTACT WITH POWER SUPPLY AND ALL OTHER POWER CABLES.

The format information on a soft-sectored diskette (used with the MF-11 system) is those sections of the disk called headers which contain track and sector numbers as described in paragraph 2.2.2.

This information may be inadvertently lost in some circumstances, or incorrectly written on a new disk by the manufacturer. In these cases, the format routine provided by the FD11-200 can be used to write this information on the diskette and recover the media. (This procedure is unlikely to help worn diskettes which give continual CRC errors)

The format routine has been placed on the control card ROM and executes under control of the 8080 microprocessor. It does not require the LSI-11 except for initialization.

CAUTION: Use of the format routing will completely erase all information which is on the diskette. Do not attempt to use it for the recovery of data.

Use this procedure to format a diskette (whether used or new):

1) Ensure the diskette to be formatted is write-enabled (see paragraph 2.2.3).
2) Remove the top cover from the MF-11 chassis (see paragraph 3.2).
3) Remove the protective cap from the toggle switch mounted on the chassis directly behind drive Ø by unscrewing it.
4) The toggle switch is used to force the drive select circuitry to select the drive you wish to use for formatting. This is a safety feature to protect media in normal use. Move the switch toward the drive you wish to use (Drive Ø is suggested).
5) Place the diskette to be formatted in the drive selected in (4), and close the drive door.
6) Set the ENABLE/HALT switch to HALT and turn POWER on (or press INIT if power is already on).
7) After the drives calibrate (about 3 seconds), use ODT from the console terminal to open the FDCS, location 177170, and deposit the format opcode 51.

   @177170 100040 51 (return) (user input underlined)

   The contents of 177170 may be ignored.

8) The unit will now step through the entire diskette writing the format (about 30 seconds). You must now use the self-test diagnostic to write data fields onto the diskette before use (proceed to paragraph 4.5.3, number 7, next).

4.5.3 SELF-TEST DIAGNOSTIC

WARNING: EXPOSED AC (See 4.5.2, WARNING).

The self-test diagnostic is a microprogram routine for checking the function of the disk drives and media. It is also used to write valid data fields on a diskette which has been formatted by the MF-11. The routine writes and then reads every sector of the diskette on all tracks and checks for valid data and format. If an error is encountered, the routine halts (activity LED on the drive goes out).

The type of error encountered is determined by examination of the control registers as described below. If no errors are encountered, the diagnostic will continue executing passes until halted by a reset command or bus INIT. The following procedure is employed:

CAUTION: The self-test diagnostic will destroy any data previously written on the diskette. Do not use it to check a data diskette for integrity. The test will fail if the disk is write-protected unless previously written with the diagnostic pattern.

1) Ensure the scratch disk to be checked is write-enabled (paragraph 2.2.3).
2) Remove the top cover from the MF-11 chassis (see paragraph 3.2).
3) Remove the protective cap from the toggle switch mounted on the chassis directly behind drive Ø by unscrewing it.
4) The toggle switch is used to force the drive select circuitry to select the drive you wish to use for checking. This is a safety feature to protect media in normal use. Move the switch toward the drive you wish to use (Drive Ø is suggested).
5) Place the diskette to be checked in the drive selected in (4), and close the drive door.
6) Set the ENABLE/HALT switch to HALT and turn POWER on (or press INIT if power is already on).
7) Using ODT, enter the FDCS address, 177170, and deposit the self test opcode, 31.

   @177170/100040 31 (return)

8) The drive will now step through each track on the drive selected, testing all sectors. It will automatically return to track Ø when it reaches the end of the disk. To halt the test, press INIT or deposit in 177170 the reset command, 40000.

If the diagnostic halts, an error has occured. The nature of this error can be found by 1 of the 2 procedures given below:

(1) Read the FDDB register (177172). If this contains a one, a CRC error has occured. A new diskette should then be tried to see if the problem is in the system or the media. Bad diskettes will often give CRC errors at the same point on the diskette each time.

(2) If the FDDB contains 0, the read error register function must be used in order to pin-point the error. The op code for the read error register function, 17, must be deposited in the FDCS, location 177170. Location 177172 may now be read and will contain an error code listed on page 5-6. The test should be repeated with new media to see if bad media has been the problem.

It should be noted that the write-protect switches are not examined by the diagnostic routine. They will prevent writing on the diskette, but they will not present a status bit. If the diagnostic is run in write-protect mode it will either: (1) show no errors if the disk has previously been written with the diagnostic pattern, or (2) show a 60 or self-diagnostic type error indicating that when reading the diskette, the information read back was not what was expected. The write-protect switch may be used to run the diagnostic routine in a read-only mode on a diskette previously written with the diagnostic pattern.

The internal diagnostic does not test all aspects of the controller card, but may be a helpful tool in locating problems and in running data reliability tests. It cannot test the Unibus logic nor certain instruction set functions.

FD11-200 DETAILED DESCRIPTION

5.1 GENERAL

The FD-11 disk system used in the MF-11 is software equivalent to an RXV11. Program control of the FD-11 is accomplished by the proper manipulation of two device registers in the FD-11. The first of these two registers, the FDCS, serves to pass control information from the CPU to the FD-11, and to report status and error information from the FD-11 to the CPU. The second register, the FDDB serves as the data path between the CPU and the FD-11. The information that is present in the FDDB at any given time is a function of the FD-11 operation that is in progress at that time.

Data transfers both to and from the diskette are always one complete sector (128 eight bit bytes) of information per transfer command. Partial sector transfers (less than 128 bytes) are not accomodated by the FD-11.

The FD-11 contains a read/write data buffer of 128 bytes. During write operations, this buffer is first loaded under program control, then the write command is issued which transfers the contents of the buffer to the diskette. During read operations the read instruction is issued and the information from the proper sector and track is read into the buffer. After the buffer is full, the contents of the buffer are read one byte at a time, into the CPU via the FDDB, under program control.

5.2 REGISTER AND VECTOR ADDRESSES

The normal address assignments for the FD-11 device registers and the interrupt vector address are as follows:

Function	Address
FDCS	177170
FDDB	177172
Interrupt Vector	264

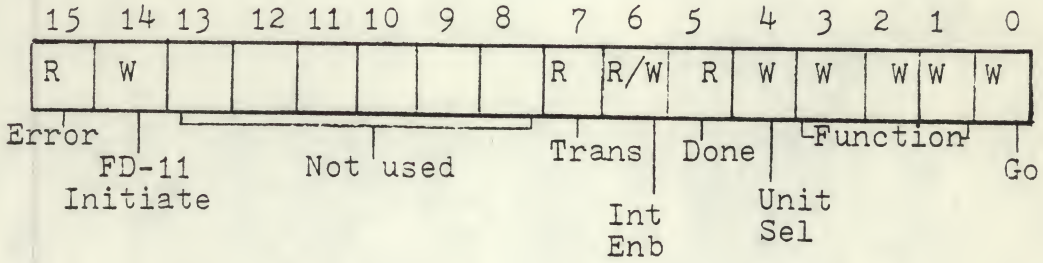
5.3 FD-11 REGISTER DESCRIPTION

The 2 registers listed above are the only data paths between the CPU and the FD-11. The first of these registers is used to initiate commands and indicate certain status information. The second of these registers has 5 different uses; which one it serves is determined by the protocol of the operation being performed. These five functions are: (1) for

transferring data to and from the 128 byte buffer in the FD-11, (2) to transfer the sector address for a read or write operation, (3) to transfer the track address for a read or write operation, (4) to indicate certain common error conditions, and (5) to indicate codes for less common errors.

5.3.1 FDCS COMMAND AND STATUS REGISTER (177170)

Commands to the FD-11 are initiated by loading this register with the proper function code accompanied by the "Go" bit provided that the FD-11 is not busy when the command is issued. The operation codes and bit assignments for the FDCS are shown below. Bits designated W are write only, bits designated R are read only, and bits designated R/W can be both written and read by the CPU.



Binary Function Code

000	Fill Buffer
001	Empty Buffer
010	Write A Sector
011	Read A Sector
100	Special Functions (see paragraph 5.4.10)
101	Read Status
110	Write Deleted Data Sector
111	Read the Error Register

Figure 5-1 FDCS Bit Assignments and Function Codes

5.3.1 FDCS COMMAND AND STATUS REGISTER (177170) continued

Description of bit assignments for FDCS

Bit number	Function
0	Go bit. Initiates the selected operation in the FD-11.
1-3	Function code. The coding of these three bits select the operation to be performed by the FD-11.
4	Unit select Bit - Selects which of two disk drives is to execute the selected operation.
5	Done Bit. Indicates the completion of an operation. If Interrupt Enable is set when Done is asserted, a program interrupt will occur.
6	Interrupt Enable. When this bit is set, the FD-11 will cause a program interrupt upon the completion of an operation.
7	Transfer Request Bit. This bit indicates to the CPU that the FD-11 requires data from the CPU or that the FD-11 contains valid data for the CPU.
8 - 13	Unused bits.
14	FD-11 Initialize. The FD-11 can be selectively initialized by setting this bit in the FDCS. Other devices connected to the system bus are not affected. The effects of setting this bit in the FDCS are: (a) Reset Done Bit (b) Move the head of drive 1 to track 0. (c) Move the head of drive 0 to track 0. (d) FD-11 clears the Error and Status Register (e) FD-11 sets Initialize Done. (f) FD-11 sets FDES bit 7 (DRV RDY) if drive 0 is ready. (g) Sector 1 of track 1 of the diskette on drive 0 is read into the buffer.

5.3.1 FDCS COMMAND AND STATUS REGISTER (177170) continued

Description of bit assignments for FDCS (continued)

Bit number	Function
15	Error. This bit indicates an error of some type occured during a command. It is cleared by a new command or an initialize.

5.3.2 FDDB REGISTER (177172)

As mentioned in paragraph 3.3, this register has five distinct functions determined by the protocol of the operation. Section 3-4 details this protocol. The FDDB can be read when the FD-11 is not executing a command. When the FD-11 is executing a command, the FDDB can be read and written only when the TR (transfer) bit (FDCS bit 7) is set.

5.3.2.1 DATA BUFFER REGISTER

This register serves as a 1 byte data path between the CPU and the FD-11 when filling or emptying the internal 128 byte buffer.

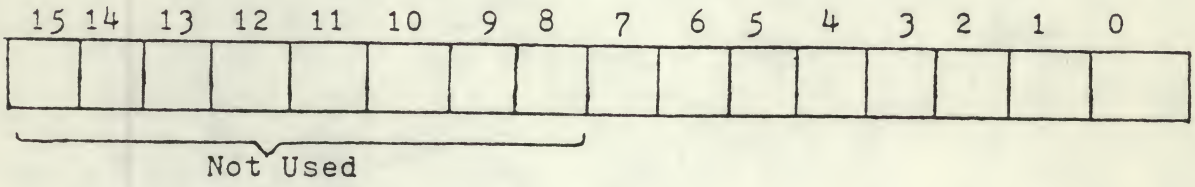


Figure 5- 2 Data Buffer Format

5.3.2.2 SECTOR ADDRESS REGISTER

This register indicates which of 26 sectors, numbered 1 through 26 (32 octal), are to be used in a read or write command.

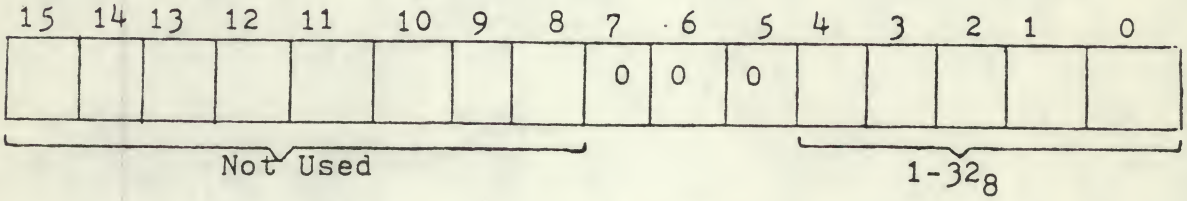


Figure 5- 3 Sector Address Format

5.3.2.3 TRACK ADDRESS REGISTER

This register indicates which of 77 tracks, numbered 0 through 76 (114 octal), are to be used in a read or write operation.

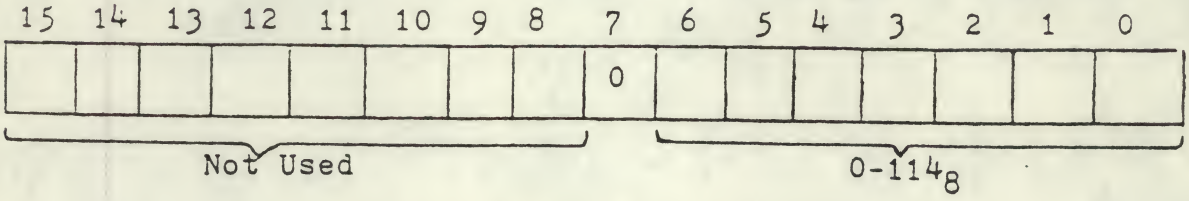


Figure 5-4 track address format.

5.3.2.4 ERROR AND STATUS REGISTER

This register contains certain error and status flags for the drive selected by the unit select bit. It is always available at the completion of an operation and may also be read by the read status function.

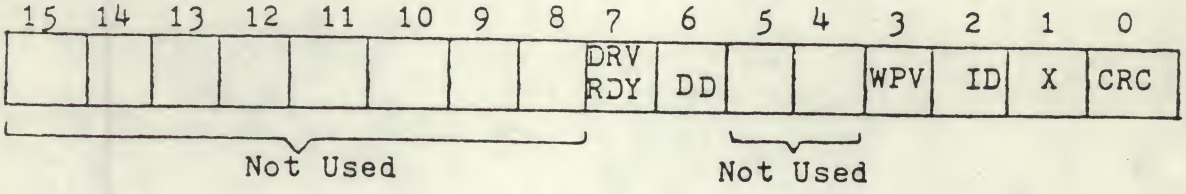


Figure 5-5 Error and Status Format

Bit No.	Code	Description
0	CRC	A cyclic redundancy error has occured in a read operation.
1	X	This is used in DEC systems to indicate a data transfer error between the 2 boards in the controller. This is not used in the FD-11 system because a single board controller design has been used.
2	ID	Initialize DONE - indicates that an initialization took place. This can be caused by a power failure, programming or a Unibus signal.

5.3.2.4 ERROR AND STATUS REGISTER (continued)

Bit No.	Code	Description
3	WPV	Write protect violation - an attempt was made to write on the diskette when the write-protect switch was set.
4 - 5		Not used.
6	DD	A deleted data mark was found during a read, or the last command issued was a write deleted data command.
7	DRV RDY	This bit indicates that the selected drive is ready and has a diskette installed correctly. It is only valid when retrieved after a Read Status function or after an initialize when it indicates the status of drive 0.

5.3.2.5 ERROR CODE REGISTER

This register should be read if the error flag (bit 15 of the FDCS) is set but no error flag can be found in the error and status register. It is accessed via the read error register function only. It will contain one of the bit codes listed below:

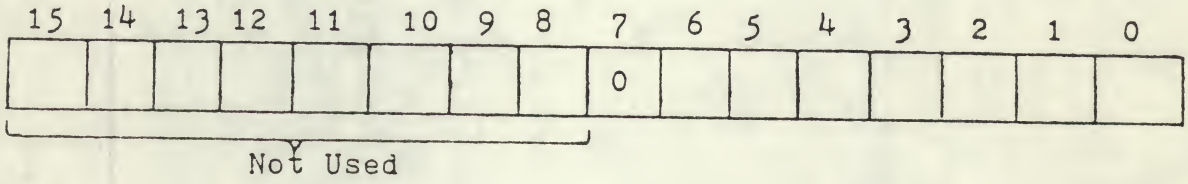


Figure 5-6 Error Code Register

Octal Code	Meaning
10	Drive 0 failed to see home on Initialize.
40	Tried to access a track greater than 77.
60	Data Error found when executing self-diagnostic
70	Desired sector could not be found after looking at 52 headers (2 revolutions).
120	A preamble could not be found.
130	Preamble found but no I/O mark found within allowable time span.
140	CRC error on what we thought was a header.
150	The header track address of a good header does not compare with the desired track.

5.4 COMMAND FUNCTIONS AND THEIR PROTOCOL

The function codes listed in Figure 3-1 are described in detail below. The specified protocol of each function must be observed or data loss may result.

5.4.1 FILL BUFFER FUNCTION (000)

This function is used to fill the FD-11 128 byte internal buffer with data from the CPU. The contents of the buffer are usually written onto the disk after completion of this operation. The following procedure is used in executing this function:

(1) Store function code 000 and Go bit into FDCS.
(2) Check for the TR bit in the FDCS set on.
(3) Now 1 byte of data may be transferred to the FDDB.
(4) Repeat steps 2 and 3 until exactly 128 bytes of data have been transferred.

The Done bit will then be set and the function is complete.

5.4.2 EMPTY BUFFER ROUTINE (001)

This function is used to empty the FD-11 128 byte internal buffer into the CPU.

This function is usually performed after the completion of a read operation. The following procedure is used in executing this function:

(1) Store function code 001 and Go bit into FDCS.
(2) Check for the TR bit in the FDCS set on.
(3) Now 1 byte of data may be transferred from the FDDB.
(4) Repeat steps 2 and 3 until exactly 128 bytes of data have been transferred. The Done bit will then be set and the function is complete.

5.4.3 WRITE SECTOR FUNCTION (010)

This function is used to write the contents of the FD-11's internal buffer onto the disk. The following procedure is used in executing this instruction.

(1) Store function code 010 and Go bit into FDCS.

5.4.3 WRITE SECTOR FUNCTION (010) (continued)

(2) Check for the TR bit in the FDCS set on.
(3) Now transfer the sector address to the FD-11 via the FDDB.
(4) Check for the TR bit set.
(5) Now transfer the track address to the FD-11 via the FDDB.
(6) On completion of the operation the Done bit will be set and the FDDB will contain the error and status register.

5.4.4 READ SECTOR FUNCTION (011)

This function is used to read a diskette sector into the FD-11's internal buffer. The procedure followed by this function is identical to that of the Write sector function described in the previous paragraph. After waiting for the TR bit each time, the sector address and then the track address are deposited into the FDDB, location 177172. The function is then executed.

5.4.5 SPECIAL FUNCTION CODE (100)

These functions are reserved for maintenance functions.

5.4.6 READ STATUS FUNCTION (101)

When this function is executed the error and status register will be loaded into the FDDB. This register will contain the same status generated from the last operation except bit 7 which will indicate whether the drive selected by the unit select bit is ready or not.

5.4.7 WRITE SECTOR WITH DELETED DATA FUNCTION (110)

This function is identical to the write sector function described in paragraph 3.4.3 except that a deleted data mark is written just before the start of the data field.

5.4.8 READ ERROR CODE REGISTER FUNCTION (111)

This function is used to retrieve the error code information for errors without a bit assignment in the error and status register. This register and the meaning of these codes is described in paragraph 3.3.2.5.After depositing this function into the FDCS register, the Done bit should then be checked for completion of this function.

5.4.8 READ ERROR CODE REGISTER FUNCTION (111) Continued

At that time the FDDB may be read and will contain an error code (if the error flag was set). Execution of this function clears bits 0 through 6 of the error and status register.

5.4.9 POWER FAIL OR CLEAR

If a power clear is generated by the console, or if the power fail signal is generated, an initialization sequence takes place. This sequence is the same as that given on page 5-3 under bit 14.

5.4.10 SPECIAL FUNCTIONS

The FD11-200 uses two codes, octal 31 and 51, for running disk diagnostics and writing format information onto a diskette under microprogram control. These codes are useful only when the processor is halted, and will not be recognized if issued under program control (octal code 11 is reserved for the FD11-100 card bootstrap feature and is not used by the FD11-200). See paragraphs 4.5.2 and 4.5.3 for instruction on using the diagnostic and formatting routines.

5.5 INTERLEAVING SECTORS

In order to gain efficient throughput, access to long data blocks should be made by interleaving sectors. Because the FD-11 is tied up with transferring data to or from its internal 128 byte buffer for every read or write of a sector, it is preferrable to access every other sector in long data transfers. The time spent in-between sectors is used for the empty or fill function.

If sectors are accessed sequentially, the extra time spent emptying or filling the 128 byte buffer will cause the FD-11 to just miss the beginning of the next sector. This results in a worst-case rotational latency each time and can reduce throughput by a factor of 10. Interleaving is built into DEC's operating systems and should be included in any user-developed operating system.

POWER SUPPLY

6.1 General

The MF-11 power supply is a multiple voltage source for all elements in the chassis box. DC voltages of -5, +5, +12, and +24 volts are supplied. Adjustments on the printed circuit card control voltage level, current limit, and over-voltage crowbar (E, I, CB; the five volt crow bar adjustment is labeled: +5CB) as identified by the on-board nomenclature).

The power supply also contains circuitry for the generation of the line time clock signal and DC power good signals.

Circuit details and connector pin-outs are shown in the schematic at the back of this manual.

6.2 Specifications

Input:

120 VAC, 60 Hz, at 4 amps, circuit breaker protected
or optionally 220 VAC, 50 Hz, at 2 amps, fused.

Outputs:

+5 VDC at 2 amps	J3, pins 5 and 6
+5 VDC at 2 amps	J4, pins 5 and 6
+5 VDC at 9 amps	J5, pins 1 and 2
+5 VDC at 9 amps	J5, pins 3 and 4

Total +5 volt draw limited at 18 amps

+12 VDC at 4 amps	J5, pins 6 and 7
+24 VDC at 2 amps	J3, pins 1 and 2
+24 VDC at 2 amps	J4, pins 1 and 2
-5 VDC at 0.5 amp	J3, pins 3 and 4
-5 VDC at 0.5 amp	J4, pins 3 and 4
-5 VDC at 0.5 amp	J5, pins 5 and 8

POK not, asserted low when all voltages compare properly with corresponding references

CLK, line frequency clock signal

6.3 Removal of Power Supply

WARNING: ALWAYS REMOVE AC PLUG FROM POWER OUTLET BEFORE REMOVING SUPPLY. POWER SUPPLY COMPONENTS MAY BE HOT AFTER OPERATION.

It may be necessary to replace or service the power supply after accident or component failure in the field. The power supply is mounted as a single module, and is easily removed.

6.3.1 Standard Backplane

1) Turn power off and disconnect line plug.
2) Remove top cover (as per Chapter 3).
3) Grasp the -5 volt connector at the FD11-200 controller card and remove it by pulling straight up. Note that the connector has a lip which must engage the card connector when replaced.
4) Remove the 4 pin connector J6 from power supply board. Note that this connector contains a blocking pin in an unused position to provide polarity.
5) Remove the keyed mate-and-lock connectors J3, J4, and J5 by pressing in on the handles and gently rocking back and forth while pulling out. Considerable effort may be required.
6) Separate the three wire AC connector by pulling it apart.
7) Remove the four power supply mounting screws from the outer surface of the enclosure side panel behind the power supply.
8) Lift the supply module straight up and out of enclosure.

Simply reverse the operation to re-install power supply. The unit is mounted with the heat sink down, transformer at the rear, and components facing the center of the chassis box.

6.3.2 Extended Backplane

Removal is the same as on 6.3.2. The supply is mounted to the enclosure with the heat sink up, transformer at the front, with components facing the center of the chassis box.

DRIVE SYSTEM MAINTENANCE

This section contains the basic maintenance information on the MF-11 needed to service the drive system (FD-11) spare parts. It is suggested that only large volume users of the MF-11 attempt to service the system to the component level. It is far better for the majority of users to swap out either a controller card or a drive in the event of a failure. We have included here the diagnostic and maintenance procedures necessary to do this.

7.1 PREVENTIVE MAINTENANCE

Though the controller card and other electronics require no preventive maintenance, all mechanical devices do. Preventive maintenance of the disk drive, however, is minimal due to the efficient design, reliability, and manner in which the unit is operated.

7.1.1 VISUAL INSPECTION

During normal operating conditions, periodically inspect the unit for signs of dirt, wear, or loose latching hardware on the handles. When servicing the unit, check all areas for signs of loose connections, abnormal wear, and dirt accumulation on the flexible disk guide.

7.1.2 CLEANLINESS

A clean disk drive, external and internal, will extend the operating life of the equipment and enchance the appearance. The importance of periodic visual inspection and normal cleanliness of the unit cannot be over-emphasized.

7.1.3 ROUTINE MAINTENANCE SCHEDULE

A systematic routine operating check is recommended. The checks should be performed in accordance with Figure 7-1.

Inspect	Check	Frequency
R/W Head	For Dirt	Every
Head Pad	For Wear	Six
Drive Belt	For Tension	Months

Figure 7-1. Routine Maintenance Schedule

WARNING: Remove AC power from the system before servicing.

7.2 DIAGNOSING THE PROBLEM

There are really only 2 basic elements in the FD-11: the controller card and the drives. It is most important to isolate the problem to one of these 2 elements. The only other possible problems are the power supply, switches, cabling, and backplane; problems with the CPU will generally be distinct from disk drive failure--they will be visible through ODT and of very different nature. The following procedures may be used to isolate a problem.

7.2.1 CHECKING POWER SUPPLY VOLTAGES

There are 3 voltages used in the FD-11 system: +5, +24, and -5 volts. +24 is used to power the drive stepper motors, -5 in the analog front end of the drive head circuitry, and +5 as a logic power supply. The -5 volts is also used in very small amounts (under 150 milliamps) by the controller card. The -5 volts can be checked by looking at an LED on the controller card near the cable connector. If the LED is on, the -5 volt supply is working.

NOTE: This LED does not indicate that the power supply is in range, it can only indicate a complete failure when off. If a power supply problem is suspected, these voltages should be checked with a meter, measuring the drop across both the LED and the dropping resister.

7.2.2 DIAGNOSTICS

The standard DEC diagnostics should be employed to verify the reliability of both media and drives. These tests are also available from Charles River Data Systems. The RXDP monitor should be used (DZQUJ-c 21- JUL-76 RXDP - XXDP RX11/RX01 MONITOR for up to 28K is the version currently in use by CRDS) if it is desired to boot the diagnostics from the floppy.

Two passes of ZRXBE0. BIC and up to 12 passes of ZRXAE0.BIC are useful in checking the hardware. These tests do normally destroy information written on the diskette, and should not be used to check the reliability of data diskettes. (These tests are called FDCARD and FDREL on the CRDS supplied diskettes.)

7.2.3 TESTING THE SYSTEM

The first test that should be run in any circumstance is to try the initialization function. When a reset function is sent to the controller, both drives will calibrate and sector 1 of track 1, unit 0 will be read. Successful completion of this function leaves the number 40 in location 177170 and 204 in location 177172. If this function fails, attempt to boot unit 1. If one unit works but not the other, a drive problem is likely. If both units fail, a controller or cabling problem is the likely cause. (Initialization is accomplished by pressing the INIT key, or cycling power, or depositing in location 177170 the code 40000).

If both drives pass this test, the diagnostic routines should be run. When running these tests be sure that the media is good. Poor media is responsible for many of the intermittent-type failures, such as CRC errors. The self-test diagnostic may also be used (paragraph 4.5.3).

Certain problems with the controller card, for example in interrupt logic, can only be found by running the DEC floppy diagnostics or running an operating system. Failures of this type usually lead to replacement of the controller card.

7.2.4 CABLING CONSIDERATIONS

It is possible for one drive in the system to hold down the daisy-chained bus and make it appear that either both drives are defective or the controller is defective. By disconnecting one of the 50 pin edge connectors from a suspect drive, a drive may be completely isolated from the system.

7.3 REPLACING A DRIVE

WARNING: Remove AC power from the system before attempting to service the unit.

If a drive is removed from the chassis in order to be serviced or replaced, the following procedure should be carefully followed:

(1) Remove AC power from the system by pulling the line plug out of the outlet and turning the processor off.

(2) Remove the top cover of the unit.

(3) The retaining plates on the top of the drives should be removed. In addition, there are two screws holding each drive in place which are accessed from beneath the enclosure. These two screws are spring mounted such that they remain attached to the enclosure after releasing the drives; you need therefore only loosen them, not remove them.

(4) The drive may now be pulled toward the rear of the unit and out.

(5) The drive should now be free of the unit and may even be operated in this condition if the edge connector of the ribbon cable is left attached to the drive's PC board (usually there is only enough slack to run one drive).

(6) To completely replace the drive, remove the edge connector and two additional connectors: the DC connector and the AC connector. Care must be taken.

The removal of the drives is necessary for any drive maintenance. The belt, the head, and the pressure pad can easily be checked after the drive is removed. Insertion of the drives is accomplished by simply reversing the above procedure. It is suggested that it is sometimes easier to insert drives with the doors closed. Placing a diskette in a drive will allow the door to close.

7.4 REPLACING THE CONTROLLER CARD

This operation is quite simple. After unplugging the card, the ribbon cable and the power cable may be easily removed. The ribbon cable may be pulled gently to remove it. Excessive force will damage the cable.

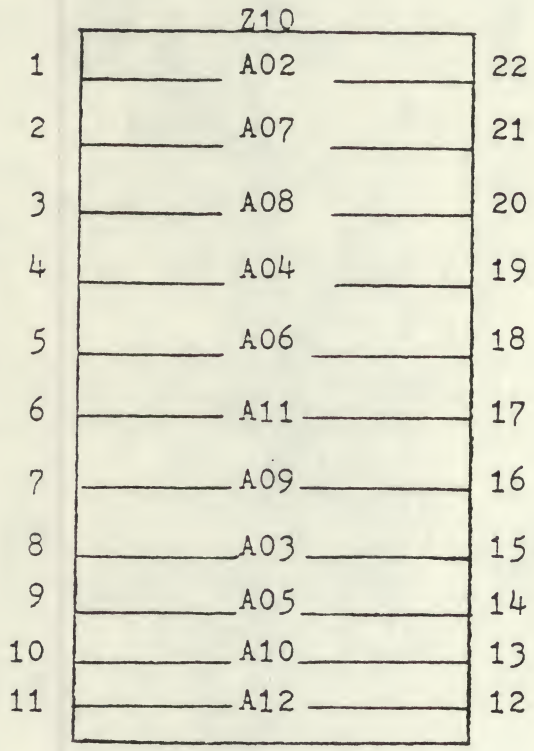
CAUTION: AC power should be removed when this operation is performed.

7.5 ADDITIONAL MAINTENANCE

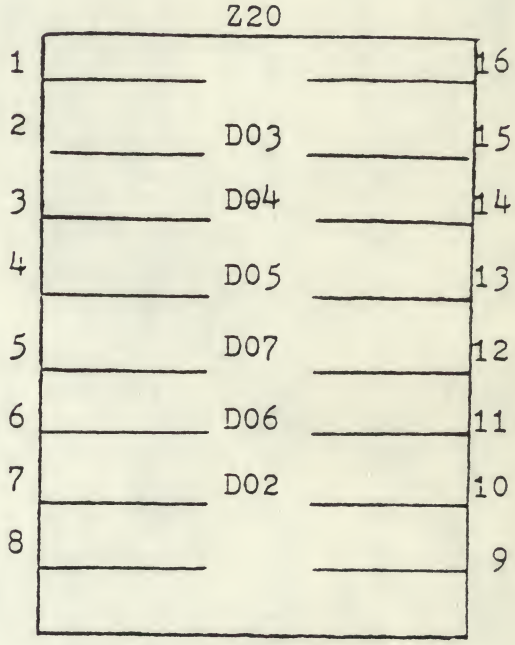
Additional information on maintenance and alignment procedures used on the disk drive is available on request.

APPENDIX A
JUMPER SELECTION GUIDE

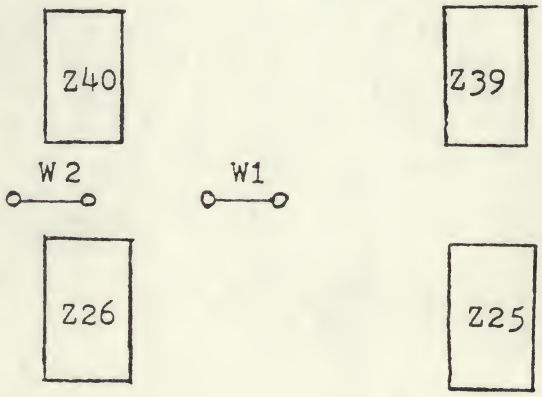
Device Address Selector

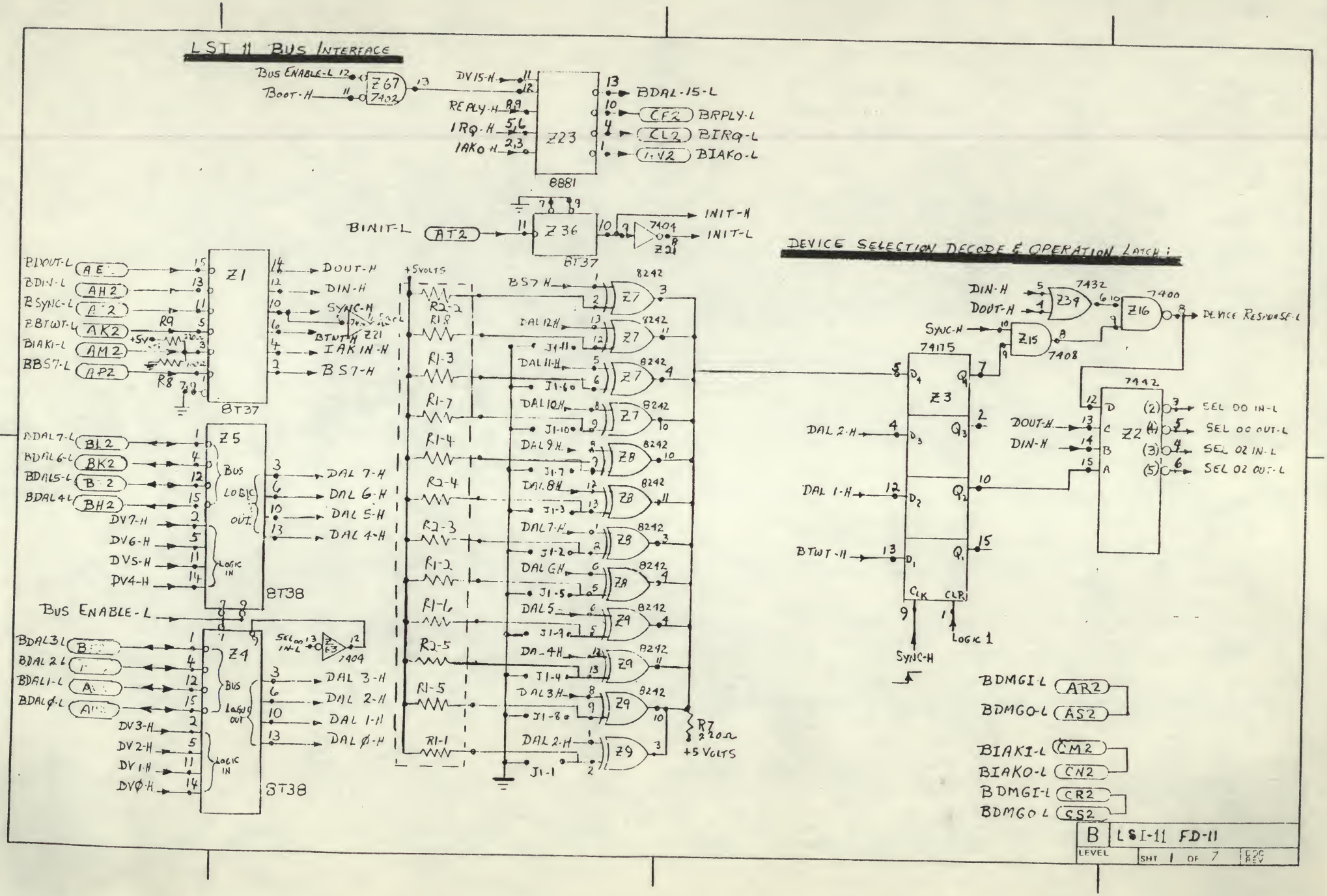


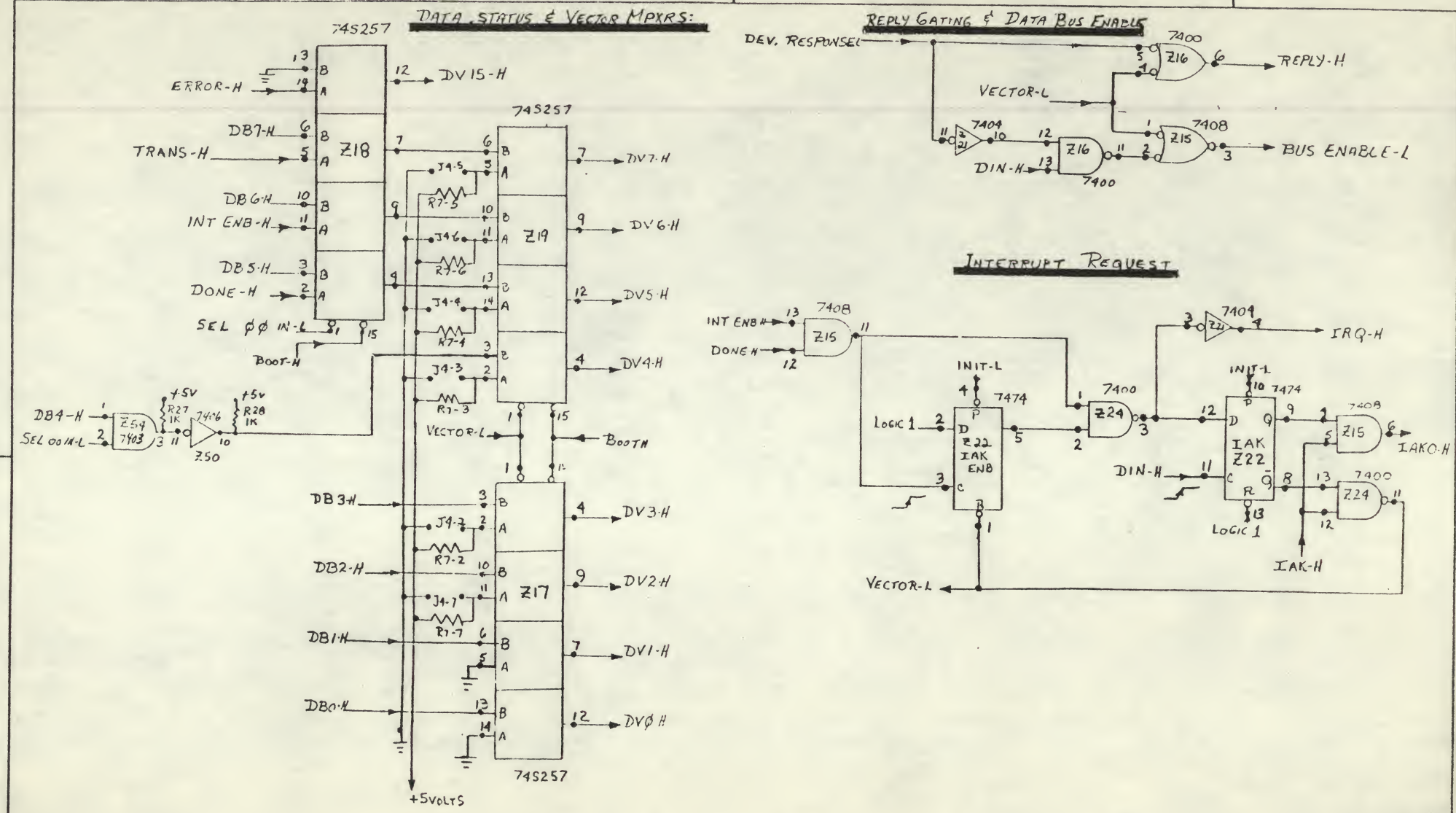
Vector Address Selector

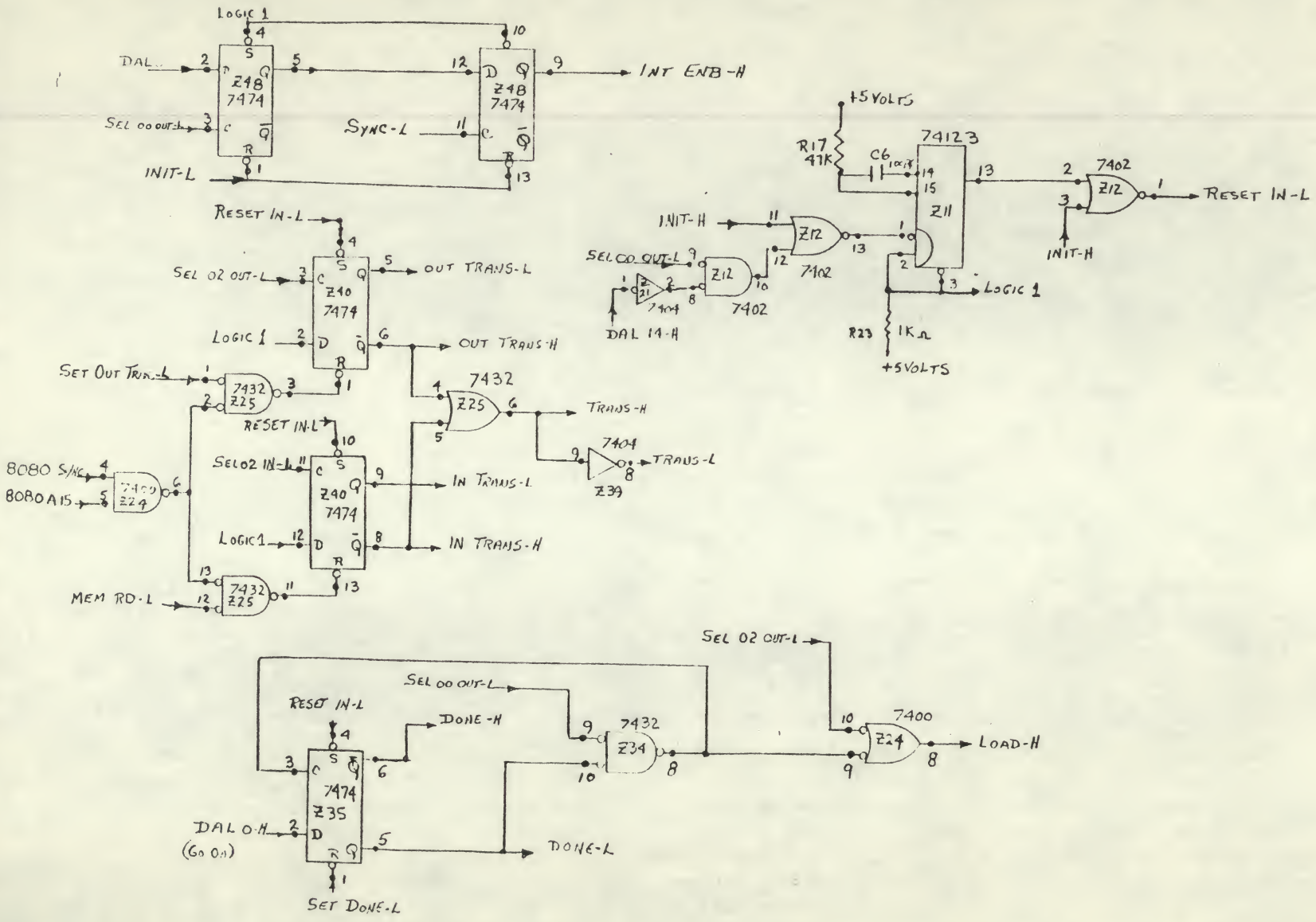


BOOTSTRAP ENABLE/DISABLE JUMPERS

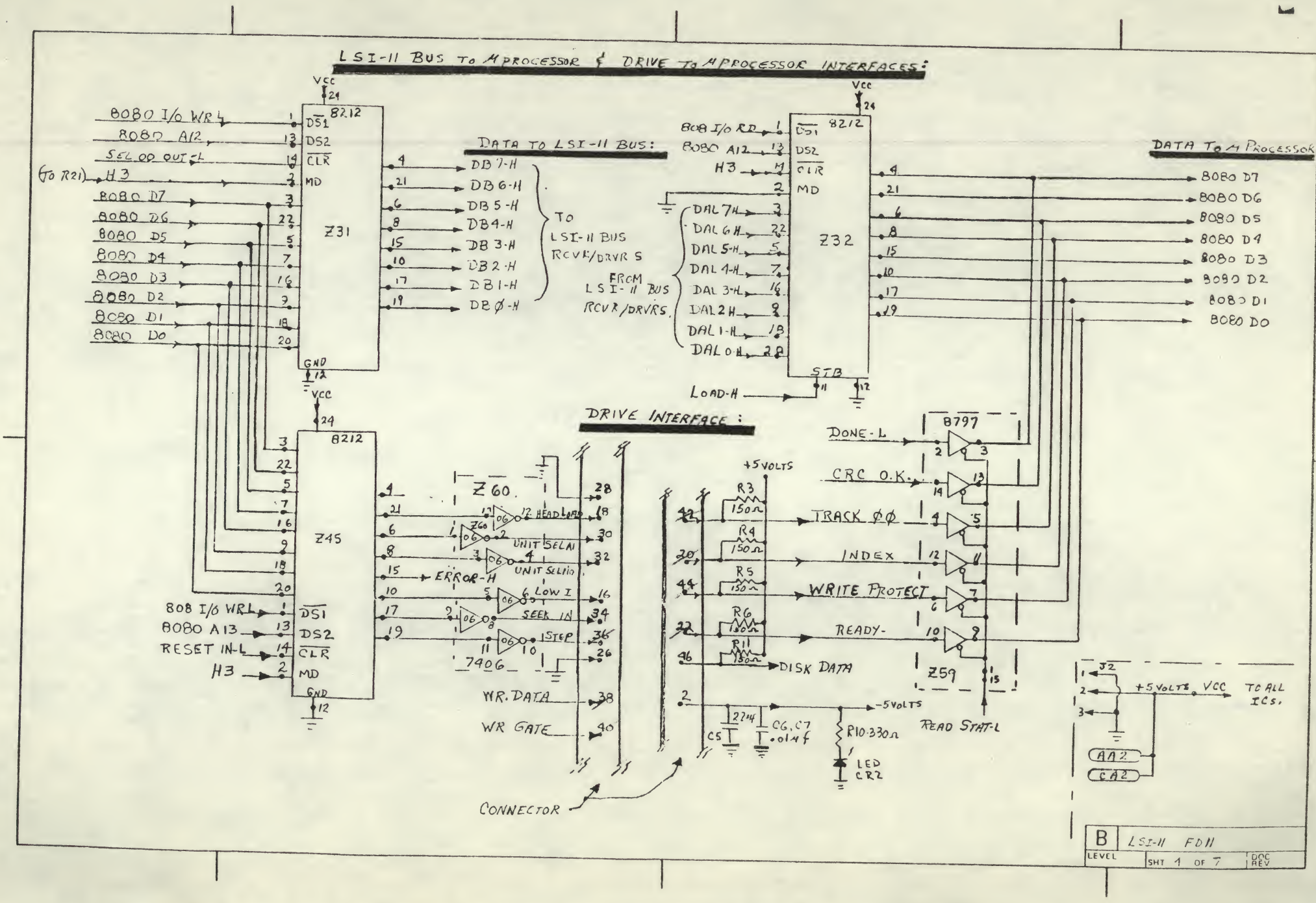


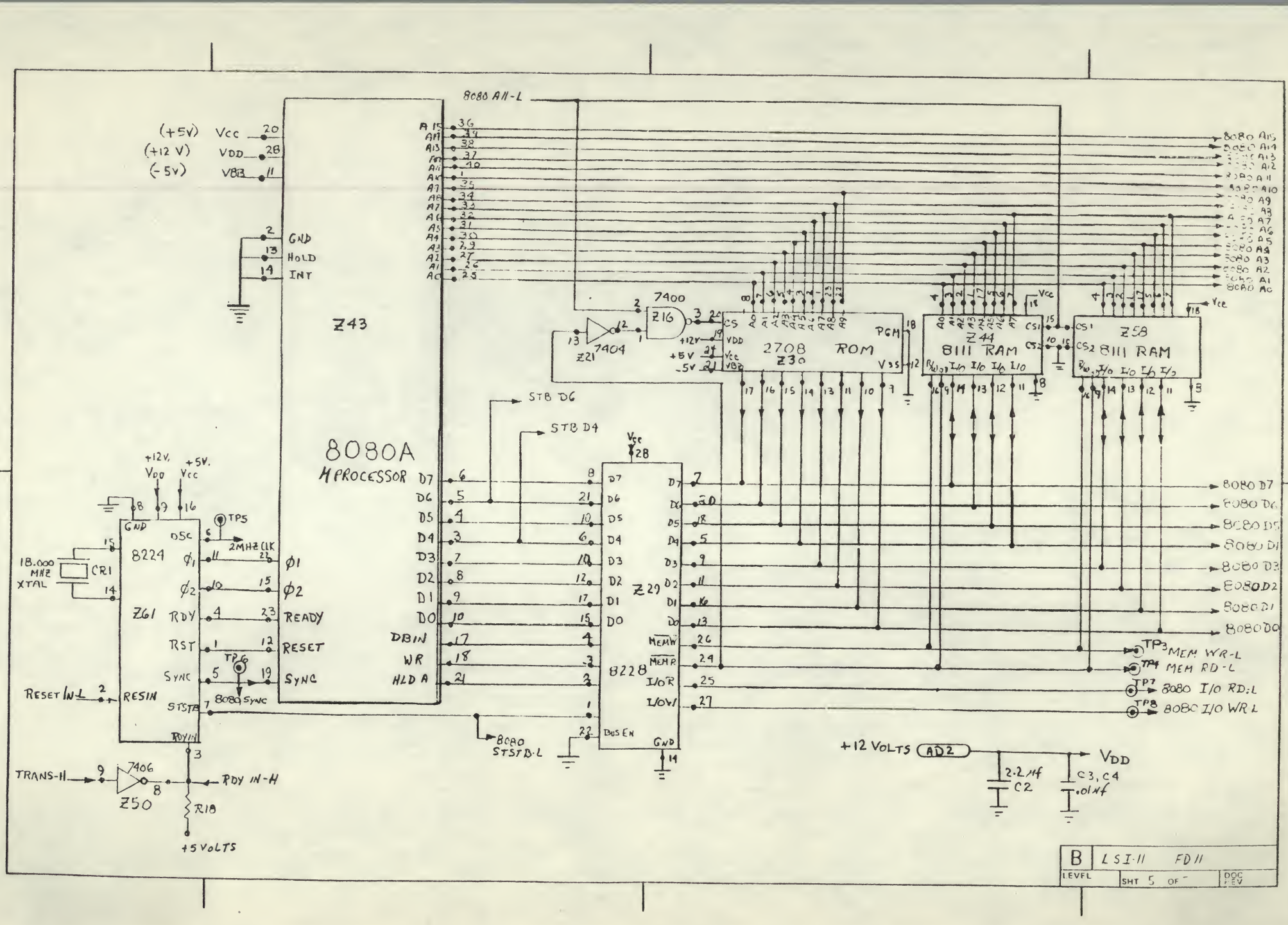

LSI 11 BUS INTERFACE
BUS ENABLE-L
BOOT-H
Z67
7402
DV15-H
REPLY-H
IRQ-H
IAKO-H
Z23
8881
BDAL-15-L
BRPLY-L
BIRQ-L
BIAKO-L
BINIT-L
AT2
Z36
BT37
7404
Z21
INIT-H
INIT-L
PDOUT-L
BDIN-L
BSYNC-L
BBTWT-L
BIAKI-L
BBS7-L
Z1
BT37
DOUT-H
DIN-H
SYNC-H
BTWT-H
IAKIN-H
BS7-H
+5VOLTS
BS7-H
DAL12-H
DAL11-H
DAL10-H
DAL9-H
DAL8-H
DAL7-H
DAL6-H
DAL5-H
DAL4-H
DAL3-H
DAL2-H
DAL1-H
8242
Z7
Z8
Z9
R2-2
R1-8
R1-3
R1-7
R1-4
R2-4
R2-3
R1-2
R1-6
R2-5
R1-5
R1-1
J1-11
J1-6
J1-10
J1-7
J1-3
J1-2
J1-5
J1-4
J1-8
J1-1
R7
220Ω
+5 VOLTS
BDAL7-L
BDAL6-L
BDAL5-L
BDAL4-L
DV7-H
DV6-H
DV5-H
DV4-H
Z5
BUS LOGIC OUT
LOGIC IN
8T38
DAL 7-H
DAL 6-H
DAL 5-H
DAL 4-H
BUS ENABLE-L
BDAL3-L
BDAL2-L
BDAL1-L
BDAL0-L
DV3-H
DV2-H
DV1-H
DV0-H
Z4
SEL00 IN-L
7409
DAL 3-H
DAL 2-H
DAL 1-H
DAL 0-H
DEVICE SELECTION DECODE & OPERATION LATCH:
DIN-H
DOUT-H
SYNC-H
7432
Z39
7400
Z16
Z15
7408
DEVICE RESPONSE-L
74175
Z3
DAL 2-H
DAL 1-H
BTWT-H
CLK
CLR
LOGIC 1
SYNC-H
7442
Z2
SEL 00 IN-L
SEL 00 OUT-L
SEL 02 IN-L
SEL 02 OUT-L
BDMGI-L
BDMGO-L
BIAKI-L
BIAKO-L
BDMGI-L
BDMGO-L
AR2
AS2
CM2
CN2
CR2
CS2
B
LSI-11 FD-11
LEVEL
SHT 1 OF 7

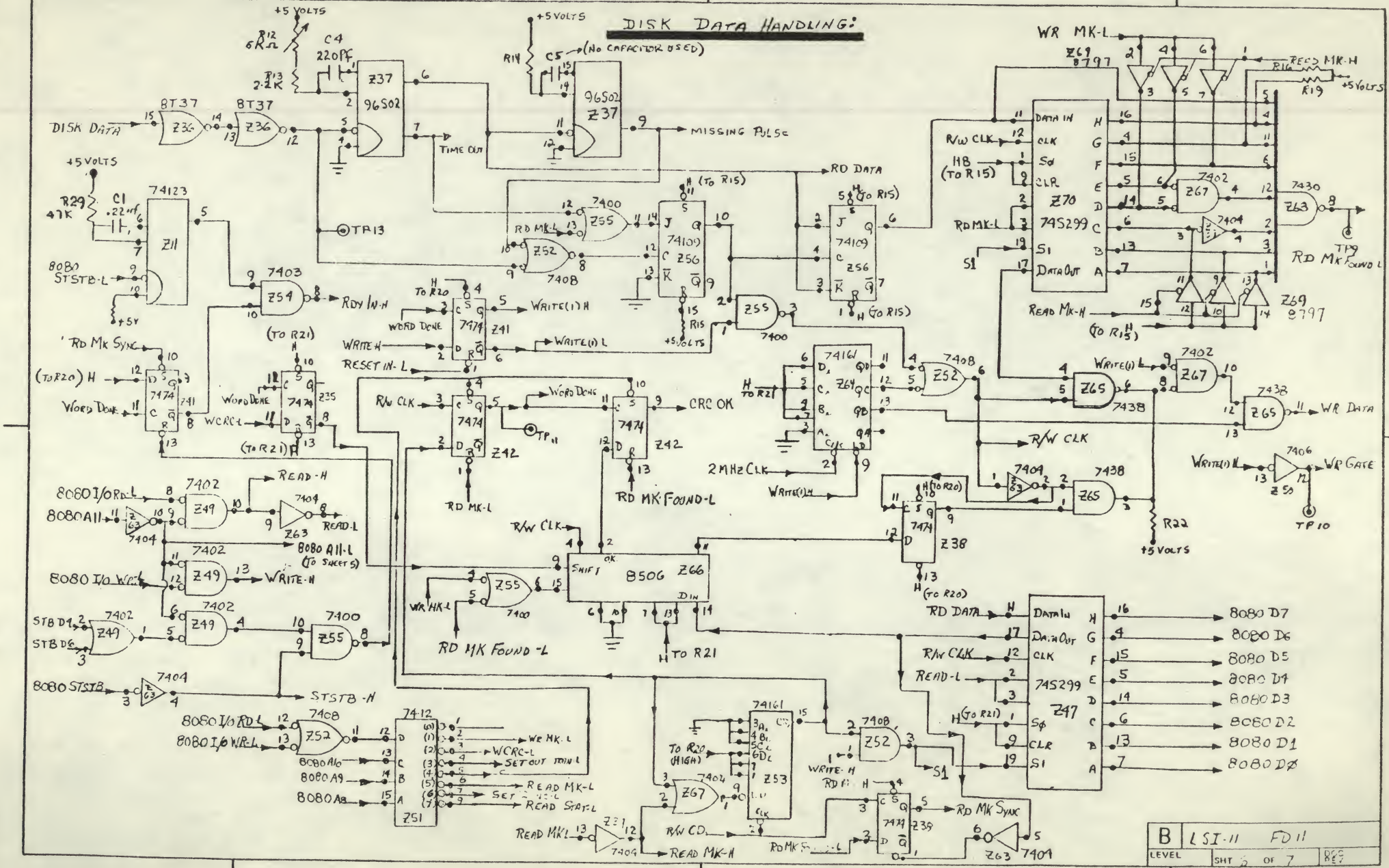

DATA, STATUS & VECTOR MPXRS:
74S257
Z18
Z19
Z17
ERROR-H
TRANS-H
DB7-H
DB6-H
INT ENB-H
DB5-H
DONE-H
SEL ØØ IN-L
BOOT-H
DV15-H
DV7-H
DV6-H
DV5-H
DV4-H
DV3-H
DV2-H
DV1-H
DVØ-H
J4-5
J4-6
J4-4
J4-3
J4-2
J4-1
R7-5
R7-6
R7-4
R7-3
R7-2
R7-1
VECTOR-L
BOOT-H
DB4-H
SEL ØØ IN-L
Z54
7403
R27 1K
R28 1K
7406
Z50
+5V
DB3-H
DB2-H
DB1-H
DB0-H
+5VOLTS
REPLY GATING & DATA BUS ENABLE
DEV. RESPONSE
VECTOR-L
DIN-H
Z16
Z15
7400
7408
7409
REPLY-H
BUS ENABLE-L
INTERRUPT REQUEST
INT ENB-H
DONE-H
INIT-L
LOGIC 1
Z22
IAK ENB
7474
Z24
IAK Z22
IRQ-H
IAKO-H
IAK-H
(DVN-H: DATA OR VECTOR BITN)
(DBNN: DATA BUFFER BITN)
(VECTOR ADDRESS IS DERIVED FROM JUMPER SETTINGS)
B
LSI-11 FD11
LEVEL
SHT 2 OF 7
DOC REV

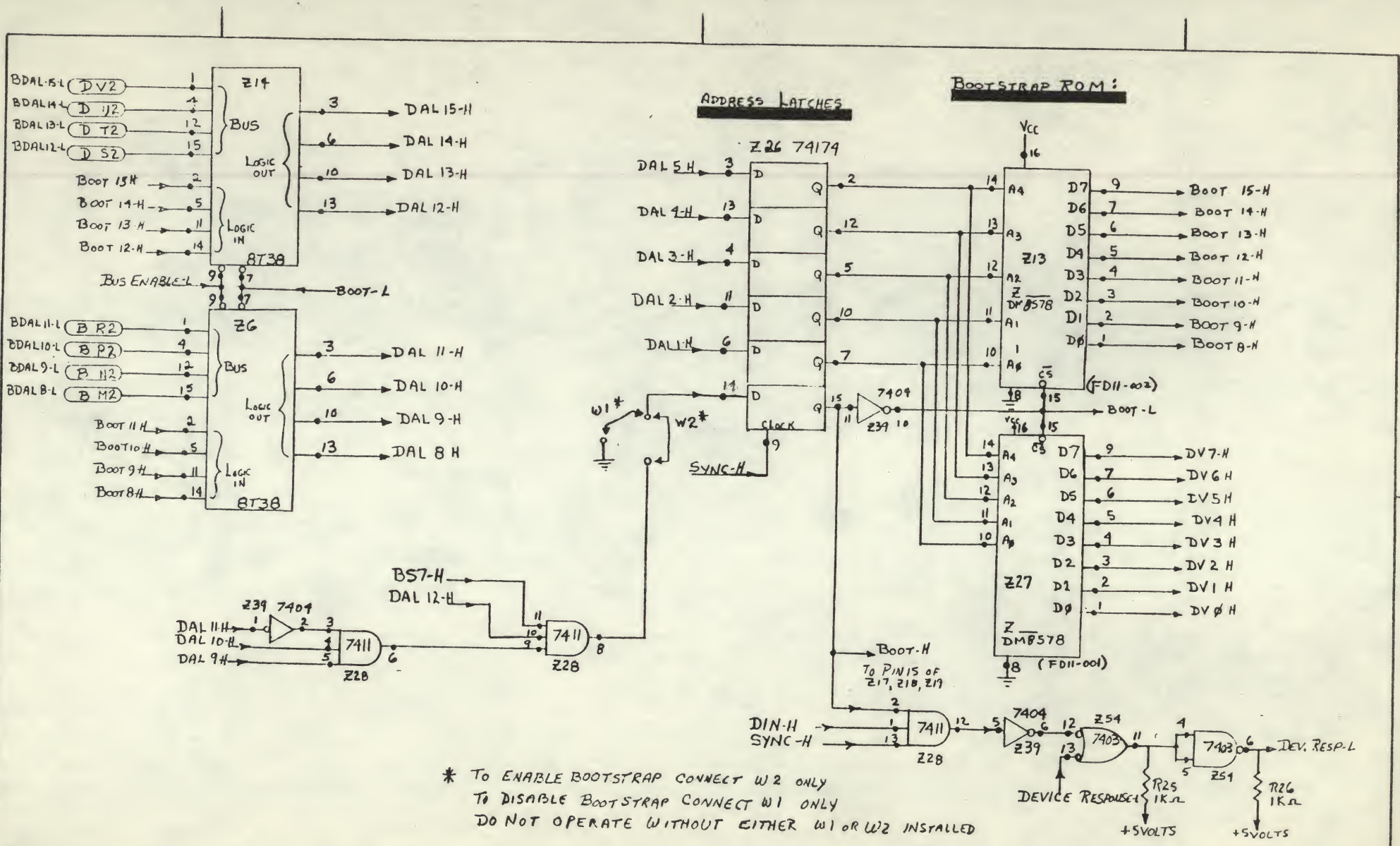


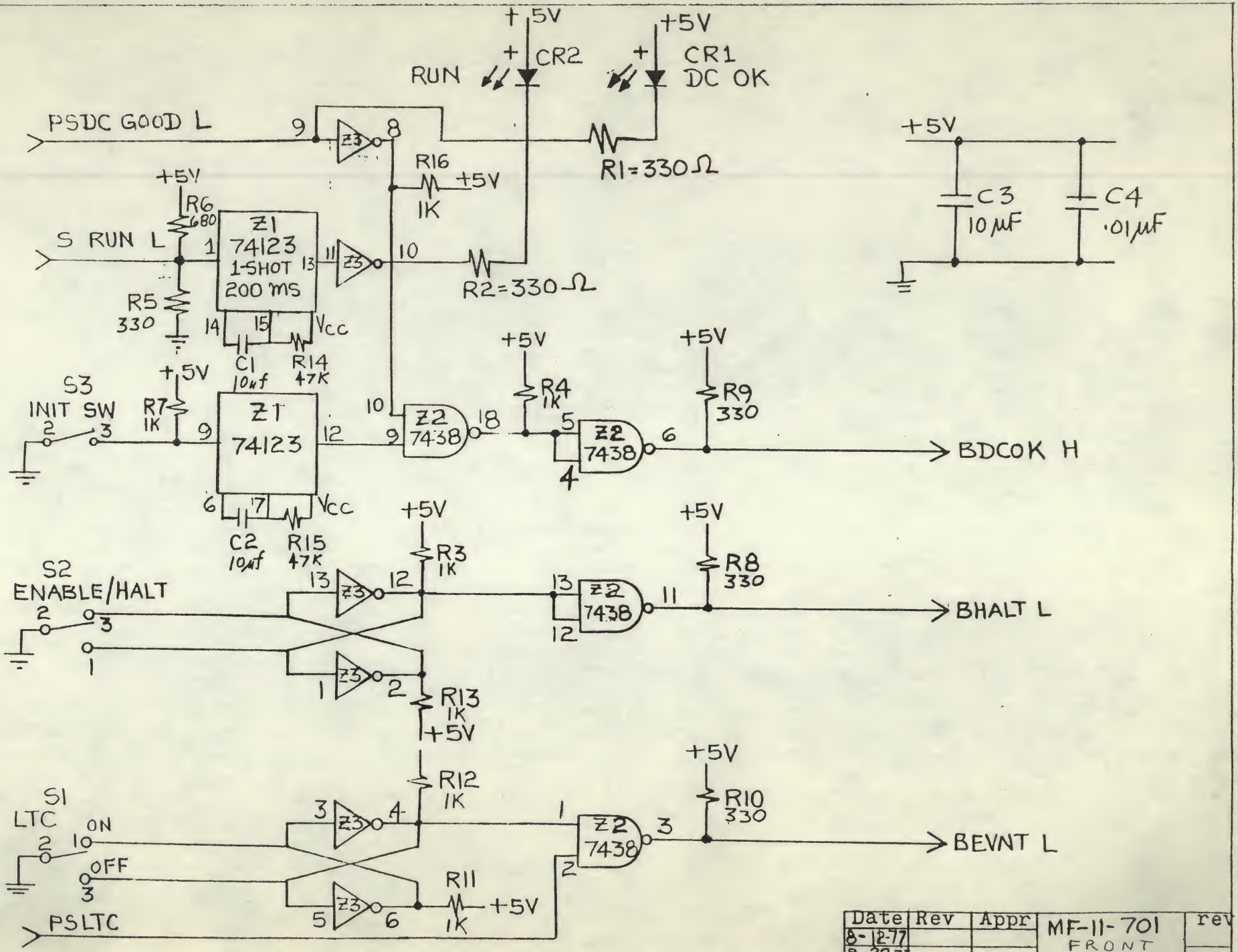
B	LSI-11 FD11	
LEVEL	SHT 3 OF 7	DOC REV


LSI-11 BUS TO μPROCESSOR & DRIVE TO μPROCESSOR INTERFACES:
8212
Z31
Z32
Z45
8080 I/O WR-L
8080 A12
SEL 00 OUT-L
(TO R21) H3
8080 D7
8080 D6
8080 D5
8080 D4
8080 D3
8080 D2
8080 D1
8080 D0
808 I/O RD
DATA TO LSI-11 BUS:
DB 7-H
DB 6-H
DB 5-H
DB4-H
DB 3-H
DB 2-H
DB 1-H
DB Ø-H
TO LSI-11 BUS RCVR/DRVRS
FROM LSI-11 BUS RCVR/DRVRS
DAL 7H
DAL 6 H
DAL 5-H
DAL 4-H
DAL 3-H
DAL 2 H
DAL 1-H
DAL 0-H
STB
LOAD-H
DATA TO μPROCESSOR
8080 D7
8080 D6
8080 D5
8080 D4
8080 D3
8080 D2
8080 D1
8080 DO
DRIVE INTERFACE:
808 I/O WR-L
8080 A13
RESET IN-L
H3
Z60
7406
HEAD LOAD
UNIT SELA1
UNIT SELB1
ERROR-H
LOW I
SEEK IN
STEP
WR. DATA
WR GATE
CONNECTOR
+5 VOLTS
R3 150Ω
R4 150Ω
R5 150Ω
R6 150Ω
R11 150Ω
DISK DATA
-5 VOLTS
C5 22μf
C6, C7 .01μf
R10 330Ω
LED CR2
8797
Z59
DONE-L
CRC O.K.
TRACK ØØ
INDEX
WRITE PROTECT
READY-
READ STAT-L
J2
+5 VOLTS
VCC
TO ALL ICs.
AA2
CA2
B
LSI-11 FDII
LEVEL
SHT 1 OF 7
DOC REV

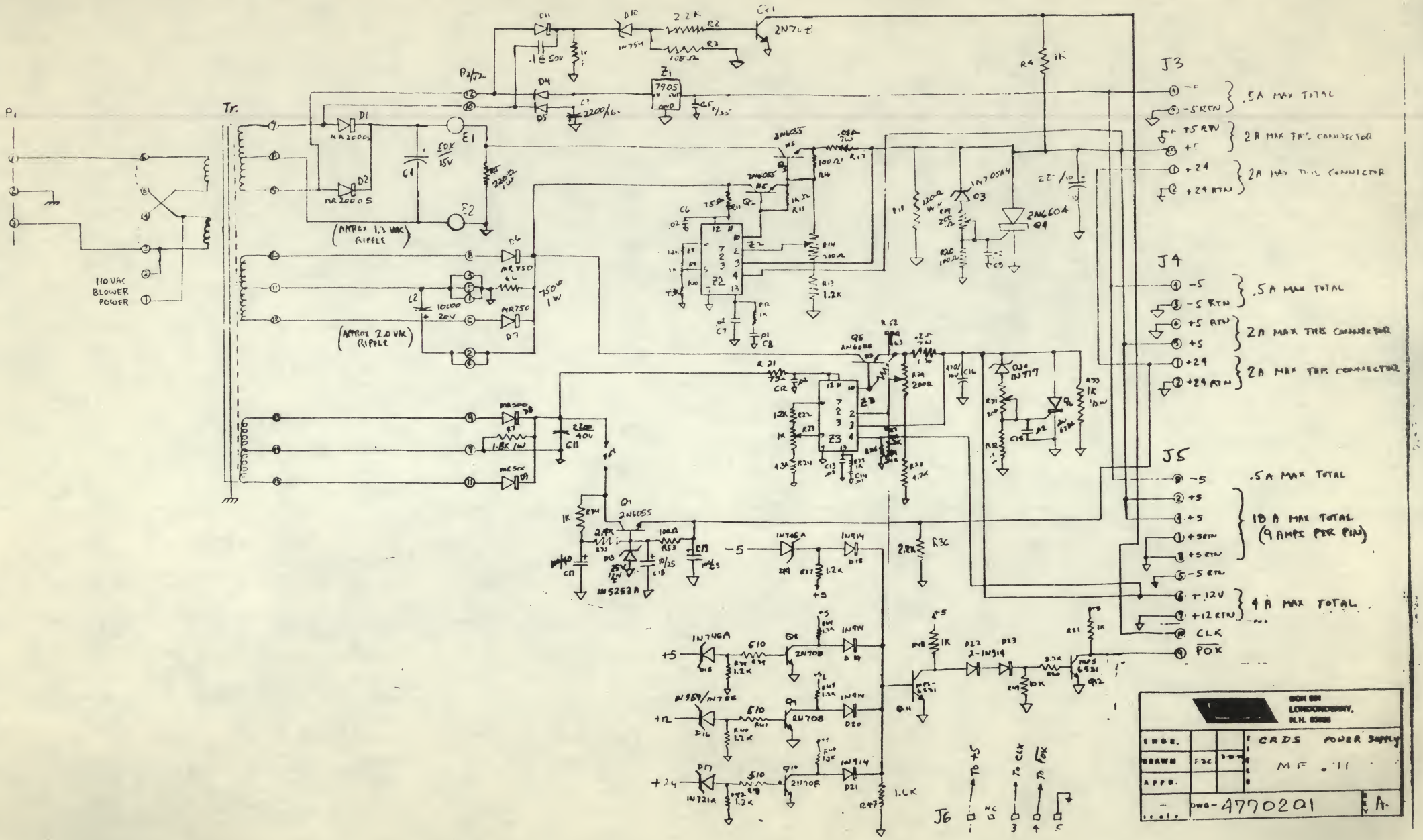

8080 A11-L
(+5V) Vcc 20
(+12 V) VDD 28
(-5V) VBB 11
GND 2
HOLD 13
INT 14
Z43
8080A
μPROCESSOR
A15 36
A14 35
A13 38
A12 37
A11 10
A10 1
A9 39
A8 34
A7 33
A6 32
A5 31
A4 30
A3 29
A2 27
A1 26
A0 25
D7 6
D6 5
D5 4
D4 3
D3 7
D2 8
D1 9
D0 10
DBIN 17
WR 18
HLD A 21
STB D6
STB D4
Vcc 28
8228
Z29
DBUS EN 22
GND 14
8080 STSTB-L
7400
Z16
7404
Z21
+12V 19
+5V 24
-5V 21
2708 ROM
Z30
PGM 18
Vss 12
Z44
8111 RAM
Z58
8111 RAM
8080 A15
8080 A14
8080 A13
8080 A12
8080 A11
8080 A10
8080 A9
8080 A8
8080 A7
8080 A6
8080 A5
8080 A4
8080 A3
8080 A2
8080 A1
8080 A0
8080 D7
8080 D6
8080 D5
8080 D4
8080 D3
8080 D2
8080 D1
8080 D0
TP3 MEM WR-L
TP4 MEM RD-L
TP7 8080 I/O RD-L
TP8 8080 I/O WR-L
+12V, VDD
+5V, Vcc
8224
Z61
GND 8
VCC 9
16
OSC 5
TP5
2MHZ CLK 23
18.000 MHZ XTAL
CR1
15
14
φ1 11
φ2 10
RDY 4
RST 1
SYNC 5
RESIN
STSTB 7
RDYIN 3
TP6
8080 SYNC
φ1 22
φ2 15
READY 23
RESET 12
SYNC 19
RESET IN-L 2
TRANS-H 9
7406
Z50
8
RDY IN-H
R18
+5 VOLTS
+12 VOLTS AD2
2.2 μf C2
C3, C4 .01 μf
VDD
B
LEVEL
LSI-11 FD11
SHT 5 OF -
DOC REV


DISK DATA HANDLING:
+5 VOLTS
R12 680Ω
R13 2.2K
C4 220PF
Z37 96S02
R14
C5 (NO CAPACITOR USED)
Z37 96S02
DISK DATA
8T37 Z36
8T37 Z36
MISSING PULSE
TIME OUT
TP13
RD DATA
R29 47K
C1 .22 MF
74123 Z11
8080 STSTB-L
+5V
7403 Z54
RDY IN-H
(TO R21)
RD MK SYNC
(TO R20) H
WORD DONE
7474 Z41
WORD DONE
WCRC-L
7474 Z35
(TO R21) H
WRITE H
RESET IN-L
WRITE(1) H
WRITE(1) L
RIS
+5 VOLTS
7400 Z55
7400 Z52
RD MK-L
7408
7400 Z55
74109 Z56
74109 Z56
(TO R15) H
R/W CLK
WORD DONE
CRC OK
TP11
7474 Z42
RD MK-L
RD MK FOUND-L
74161 Z64
2 MHz CLK
WRITE(1) H
7408 Z52
WRITE(1) L
7402 Z67
7438 Z65
WR DATA
R/W CLK
7409
7438 Z65
R22
+5 VOLTS
WRITE(1) L
7406 Z50
WR GATE
TP10
8080 I/O RD-L
8080 A11
7402 Z49
7404 Z63
READ-H
READ-L
8080 A11-L (TO SHEET 5)
8080 I/O WR-L
7402 Z49
WRITE-H
STB D1
STB D6
7402 Z49
7400 Z55
8080 STSTB
7404 Z63
STSTB-H
8506 Z66
SHIFT
DIN
OK
WR MK-L
RD MK FOUND-L
TO R21
(TO R20)
8080 I/O RD-L
8080 I/O WR-L
7408 Z52
74-12 Z51
WR MK-L
WCRC-L
SET OUT TRIN L
READ MK-L
SET
READ STAT-L
8080 A10
8080 A9
8080 A8
74161 Z53
TO R20 (HIGH)
7404 Z67
R/W CD
READ MK-L
READ MK-H
7404 Z31
RD MK SYNC
7474 Z39
7409 Z63
7404
WRITE-H
RD DATA
R/W CLK
READ-L
(TO R21)
S1
74S299 Z47
DATA IN
DATA OUT
CLK
S0
CLR
S1
8080 D7
8080 D6
8080 D5
8080 D4
8080 D3
8080 D2
8080 D1
8080 D0
WR MK-L
REQ MK-H
R18
R19
+5 VOLTS
R/W CLK
HB (TO R15)
RD MK-L
S1
74S299 Z70
DATA IN
CLK
S0
CLR
S1
DATA OUT
READ MK-H
(TO R15)
Z69 8797
Z69 8797
7402 Z67
7404
7430 Z63
TP9
RD MK FOUND L
B
LSI-11 FD11
LEVEL
SHT 5 OF 7
REV


BOOTSTRAP ROM:
ADDRESS LATCHES
Z14
BUS
LOGIC OUT
LOGIC IN
8T38
BDAL 15-L
BDAL 14-L
BDAL 13-L
BDAL 12-L
BOOT 15-H
BOOT 14-H
BOOT 13-H
BOOT 12-H
BUS ENABLE-L
BOOT-L
Z6
BDAL 11-L
BDAL 10-L
BDAL 9-L
BDAL 8-L
BOOT 11-H
BOOT 10-H
BOOT 9-H
BOOT 8-H
DAL 11-H
DAL 10-H
DAL 9-H
DAL 8 H
Z26 74174
DAL 5 H
DAL 4-H
DAL 3-H
DAL 2-H
DAL 1-H
CLOCK
SYNC-H
W1*
W2*
Z13
Z DMB578
(FD11-002)
BOOT 15-H
BOOT 14-H
BOOT 13-H
BOOT 12-H
BOOT 11-H
BOOT 10-H
BOOT 9-H
BOOT 8-H
BOOT-L
7404
Z39
Z27
(FD11-001)
DV7-H
DV6 H
DV5 H
DV4 H
DV3 H
DV2 H
DV1 H
DV Ø H
BS7-H
DAL 12-H
DAL 11-H
DAL 10-H
DAL 9-H
7411
Z28
BOOT-H
TO PINS OF Z17, Z18, Z19
DIN-H
SYNC-H
7403
Z54
Z51
DEV. RESP-L
DEVICE RESPONSE
R25 1KΩ
R26 1KΩ
+5VOLTS
+5VOLTS
* TO ENABLE BOOTSTRAP CONNECT W2 ONLY
TO DISABLE BOOTSTRAP CONNECT W1 ONLY
DO NOT OPERATE WITHOUT EITHER W1 OR W2 INSTALLED
B
LSI 11 FD-11
LEVEL
SHT 7 OF 7
DOC REV



Date	Rev	Appr	MF-11-701 FRONT PANEL	rev
8-12-77				
8-22-77				


P1
Tr.
110 VAC BLOWER POWER
(APPROX 1.3 VAC RIPPLE)
(APPROX 2.0 VAC RIPPLE)
J3
.5A MAX TOTAL
2A MAX THIS CONNECTOR
2A MAX THIS CONNECTOR
J4
.5A MAX TOTAL
2A MAX THIS CONNECTOR
2A MAX THIS CONNECTOR
J5
.5A MAX TOTAL
10 A MAX TOTAL (9 AMPS PER PIN)
4 A MAX TOTAL
CLK
POK
J6
CARDS POWER SUPPLY
MF-11
DWG-4770201
A